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Design and Implementation of Flash Analog to digital Converter

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Abstract

This paper presents the power efficient and high speed novel flash analog to digital converter. The present research uses a dynamic double tail comparator and efficient low power encoding scheme intended of ultra high frequency range (GHz) for 5-bit flash analog to digital converter. The adapted comparator is having facilities of low voltages and high sampling rate frequencies. Output of comparator block i.e. thermometer code to binary conversion block is more important because it consumes more power and speed of the circuit rebates. An encoder block in this paper is converting the thermometer code into the intermediate gray code using the merged DCVSL technique and gray code to binary code using Ex-OR logic block. The conversion of thermometer code to gray code used to rebate the bubble errors in the flash ADC. To maintain the low power dissipation with high speed, the implementation of the encoder is Merged DCVSLPG logic is presented in this paper. The used comparator and encoder implemented on CADENCE tool in 65nm technology with 0.8 V power supply. The simulation results of flash analog to digital converter average power consumption and delay is 16.33 mw and 1.542 ps. The power delay product (PDP) or Figure of merit (FOM) of the flash ADC is 25.18 fJ.

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Keywords: Analog to digital converter; Flash ADC; Merged DCVSL; Pass transistor gate logic; Ex-OR gate; Gray to Binary Logic.

1. Introduction

The main aim of this paper to rebates the power for low to medium resolution flash ADC. Low to medium resolution flash ADC has consuming more power. The consumption of more power has rebates in this paper using the modified logics of comparator and encoder blocks explained in part2. Flash ADC is the fastest ADC compared to remaining all the ADCs. The flash ADC can be used in the digital Oscilloscopes, radar, high density disk drives, communication systems and real world wireless and wire line applications.

Figure1. Illustrate the block diagram of flash Analog to Digital Comparator. The flash ADC architecture consists of 2^N -1 number of comparators and the 2^N -1 x N encoder is also required for converting the thermometer code to binary code. Each comparator requires the reference voltage and it is given by the external source and for a resistor

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divider circuit is required for dividing the largest reference voltage to the smallest reference voltage. Common analog input is giving to all the comparators. Comparator will do the comparison of analog input voltage with reference voltage if analog input is greater than the reference voltage then output voltage will be equal to '1' otherwise output voltage is '0'. This paper explains the dynamic double tail comparator [1] and merged differential cascade switch voltage pass transistor gate logic (MDCVSPGL) [4] [5]. This research work has implemented the 5-bit ADC consists of 31 comparators and the output of comparator blocks i.e. thermo meter code to gray code and gray to binary code conversion [1]. Encoder blocks implementation done in different ways. They are Wallace tree encoder [15], multiplexer based encoder [13, 17], ROM encoder [11, 12], and fat tree encoder [14] and transistor logics like DCVSL [1], current mode logic [3], pseudo MOS logic [16] etc. However comparator has to design the low power and high speed in Ultra high frequency applications (GHz). This paper is implementing the encoder block for reducing the bubble and Meta stability errors [2].

The modified dynamic double comparator is operating with ultra high frequencies (GHz) [6] and it is more energy efficient [10]. Encoder is designed using merged DCVSL pass transistor gate logic for achieving highest speed and low power dissipation with respect to other logical circuits. The design of the comparator and encoder using merged DCVSL pass transistor logic style with detailed description is presented in the part 2. The implementation of the comparator and encoder adapting merged DCVSL pass transistor logic style is presented in part 3. Simulation results and conclusion are provided in the subsequent parts.

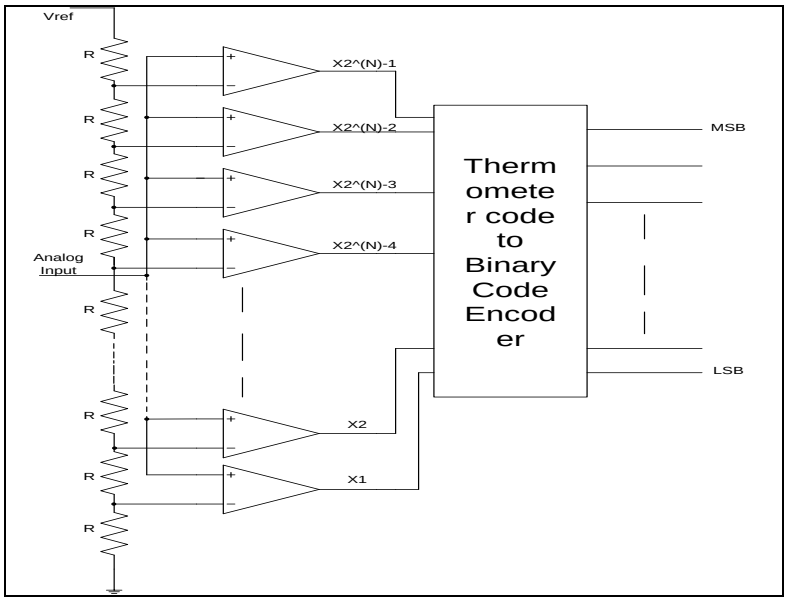

Figure 1. Block Diagram of Flash Analog to Digital Converter

2. Design of Comparator and Encoder

The comparator design is more important for the flash ADC. Here comparator designed for the application of low power and low propagation delay (high speed) and in ultra high frequency applications like GHz of sampling frequency. Here better performance low offset and low voltage comparator has modified form used in the flash ADC. Here modifications done in the input differential stage and output latch stage.

2.1. Design of a Modified comparator

The modified Comparator is shown in the below Figure2. The operation of the modified comparator of figure2 is consists of two stages. One is reset phase and other is comparison of input of voltages (evaluation phase). During

reset phase, CLK = 0, the tail transistors Mtail1, Mtail2, Ms1 and Ms2 are OFF state. The static power consumption of the circuit is reduces because of the transistors Ms1 and Ms2 are OFF. M3, M4 are ON state so V_{dd} pulls to both f1 and f2 nodes so both the transistors M11 and M12 are ON. Both outputs are tends to zero state due to the reset transistors of M5 and M6.

During the comparison of input voltages stage, CLK = V_{dd} Mtail1 and Matil2 are ON state. Transistors Ms1 and Ms2 are ON state. Transistors M3, M4 are OFF state. At the beginning of the comparison of input voltages stage, f1 and f2 nodes are full charged to V_{dd}, the control transistors are OFF state. Discharge path of the nodes f1 and f2 based on the input voltages. Suppose INP > INN then f1 discharges faster than the node f2. As long as the discharge path of the node f1 continues to falling then the control transistor Mc2 is in ON state so f2 is completely charged to V_{dd}. The control transistor Mc1 is permanent OFF state in this condition. Due to the nodes f1 is discharge to zero and f2 is charge to V_{dd} the corresponding transistor in the latch side M11 is OFF and M12 is ON condition so outp node is charged to V_{dd} and the outn node is discharged to V_{ss}. The NMOS transistors Ms1 and Ms2 are used for the reduction of static power consumption. The NMOS transistors M11 and M12 are used in the output stage for the reducing the dynamic power consumption of the total comparator circuit. These transistors are used for the connection between latch and output stages.

The positive feedback used in the differential amplifier stage for reducing the gain of circuit and increase the stability of the circuit. The modified comparator is energy efficient dynamic double tail comparator.

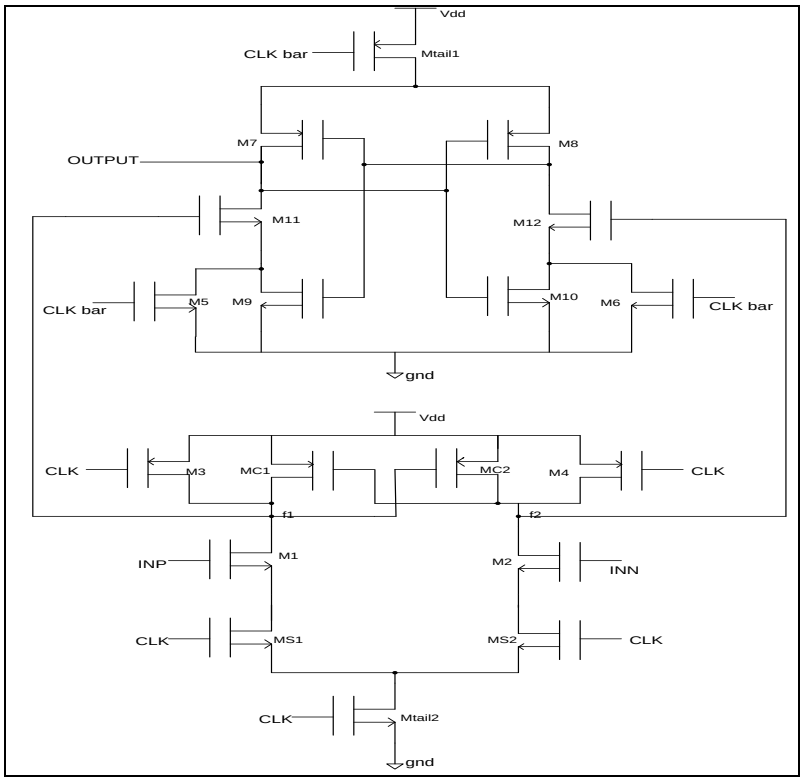

Figure 2. Modified Dynamic Double tail Comparator

2.2. Design of Implemented Encoder

Encoder block design is as shown in the figure3. The operation of the circuit is consists of two stages. One is reset phase and other is inputs assessment phase. In the reset phase (CLK= '0') the transistors M1, M2 are ON state so both the output nodes charged to V_{dd} , the transistors M5 and M6 are in OFF state and no path exist from the

ground to the supply. Since the transistors M5, M6 are in OFF condition then there is no chance to occur the static power consumption.

If the inputs are operating in assessment phase (CLK= V_{dd}) so the transistors M1, M2 are in OFF state and the M5, M6 transistors are in ON condition and the path exist between ground to supply. It depends on the inputs transistors resistance and the ON transistor M7 resistance. The path exists in the smaller resistance way between grounds to supply. The voltages of out and outb depends on the input magnitude.

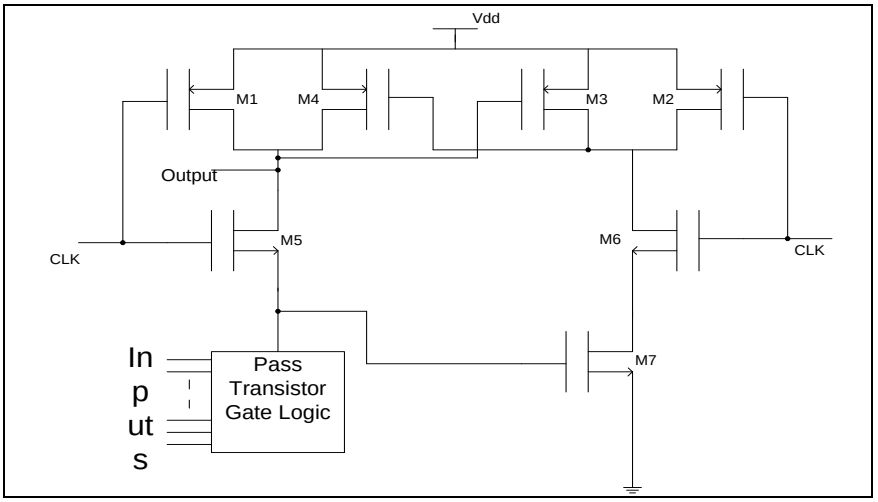

Figure 3. Encoder logic design used for flash ADC (MDCVSL PG)

3. Implementation of Modified Comparator and Encoder

3.1. Modified Comparator

Schematic diagram and transient response of modified comparator is shown in figure 4 and 5 respectively.

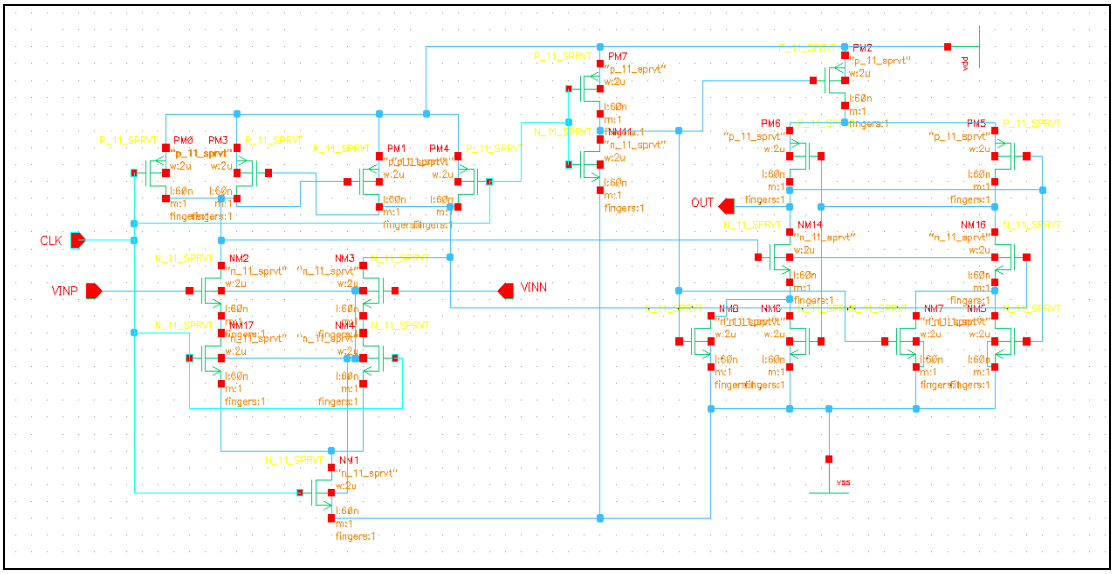

Figure 4. Schematic Diagram of Modified Comparator

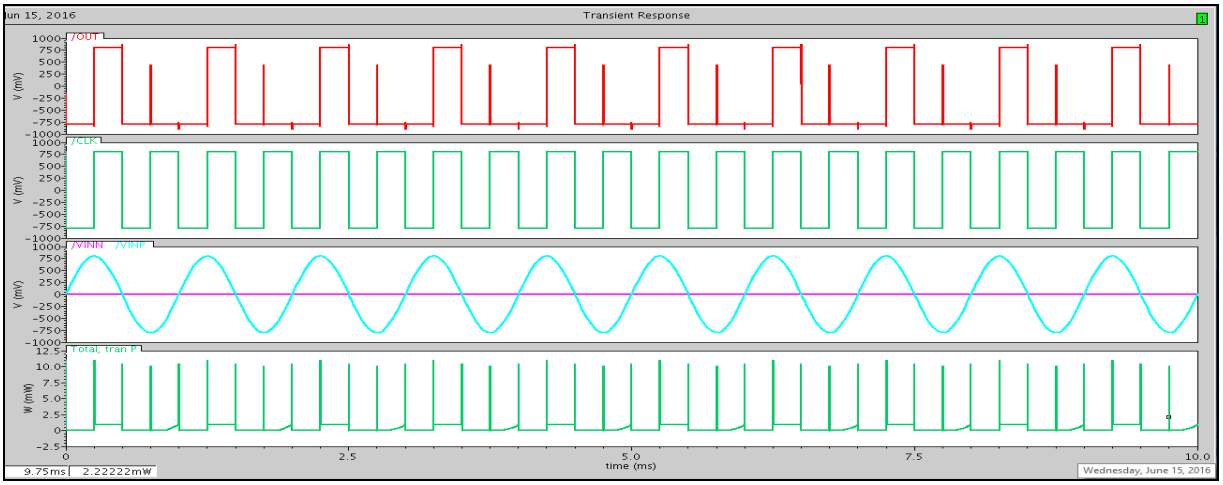

Figure 5. Transient Response of Modified Comparator

3.2. Implemented Encoder Block

The Implemented Encoder block is converts the thermometer code to intermediate gray code and gray code to binary code [1]. The thermometer code to gray code truth table and its expressions are shown below table1. Table1 shows the output of comparator block to gray code conversion logic truth table using this table we converted logical expressions are as shown in the below of table1.

Table 1. Thermometer to Gray code

G4	G3	G2	G1	G0	Thermometer Code
0	0	0	0	0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0	0	0	0	1	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1
0	0	0	1	1	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1
0	0	0	1	0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1
0	0	1	1	0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1
0	0	1	1	1	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1
0	0	1	0	1	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1
0	0	1	0	0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1
0	1	1	0	0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1
0	1	1	0	1	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1
0	1	1	1	1	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1
0	1	1	1	0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1
0	1	0	1	0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1
0	1	0	1	1	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1
0	1	0	0	1	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1
0	1	0	0	0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1	1	0	0	0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1	1	0	0	1	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1	1	0	1	1	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1	1	0	1	0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

1	1	1	1	0	00000000000011111111111111111111111
1	1	1	1	1	00000000000111111111111111111111111
1	1	1	0	1	00000000001111111111111111111111111
1	1	1	0	0	00000000011111111111111111111111111
1	0	1	0	0	00000001111111111111111111111111111
1	0	1	0	1	00000011111111111111111111111111111
1	0	1	1	1	00000111111111111111111111111111111
1	0	1	1	0	00001111111111111111111111111111111
1	0	0	1	0	00011111111111111111111111111111111
1	0	0	1	1	00111111111111111111111111111111111
1	0	0	0	1	01111111111111111111111111111111111
1	0	0	0	0	11111111111111111111111111111111111

$G_4 = I_{15}$

$G_3 = I_7 \bar{I}_{23}$

$G_2 = I_3 \bar{I}_{11} + I_{19} \bar{I}_{27}$

$G_1 = I_1 \bar{I}_5 + I_9 \bar{I}_{13} + I_{17} \bar{I}_{21} + I_{25} \bar{I}_{29}$

$G_0 = I_0 \bar{I}_2 + I_4 \bar{I}_6 + I_8 \bar{I}_{10} + I_{12} \bar{I}_{14} + I_{16} \bar{I}_{18} + I_{20} \bar{I}_{22} + I_{24} \bar{I}_{26} + I_{28} \bar{I}_{30}$

Gray to binary conversion logical expressions are shown in the below.

$B_4 = G_4$

$B_3 = G_3 \oplus B_4$

$B_2 = G_2 \oplus B_3$

$B_1 = G_1 \oplus B_2$

$B_0 = G_0 \oplus B_1$

There are different logic styles to implement the encoder design. Encoder can be designed by using the following techniques like Wallace tree encoder [15], ROM encoder [11, 12], fat tree encoder [14] and multiplexer [13]. Encoder can also design by using the various CMOS techniques like pseudo NMOS logic, dynamic and DCVSL etc. in order to rebate the static power consumption and boost up the speed of an ADC. The encoder block implemented by adapting the logic Merged DCVSPGL [4] [5]. This encoder design reduces the static power consumption and boost up the speed of the encoder block. The implemented logic is also uses the less number of transistors compared to the other techniques like pseudo NMOS, dynamic logic style and Differential cascode switch logic (DCVSL) etc. the used technique of encoder adapts the positive feedback to boost the stability of the network to more. The logical expressions are designed using the pass transistor. Pass transistor technique the boost up the speed and rebates the power consumption [5]. The pass transistor OR and AND gates are shown in figure 6 and figure7.

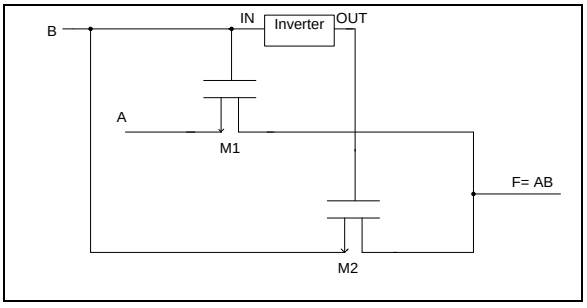

Figure 6. Pass transistor AND gate

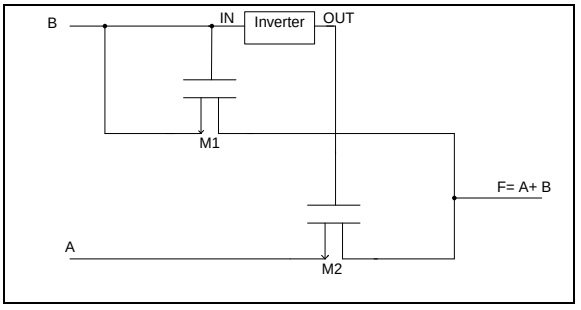

Figure 7. Pass transistor OR gate

3.2.1. Schematic Diagrams of Thermometer to gray code Conversion

The schematic diagrams of the thermometer code to gray code conversion logical diagrams for different bits are as shown in below figure 8 and its transient response is as shown in the figure 9. Logical expression expressed using the pass transistor logics are as shown in the above figure 6 and figure7.

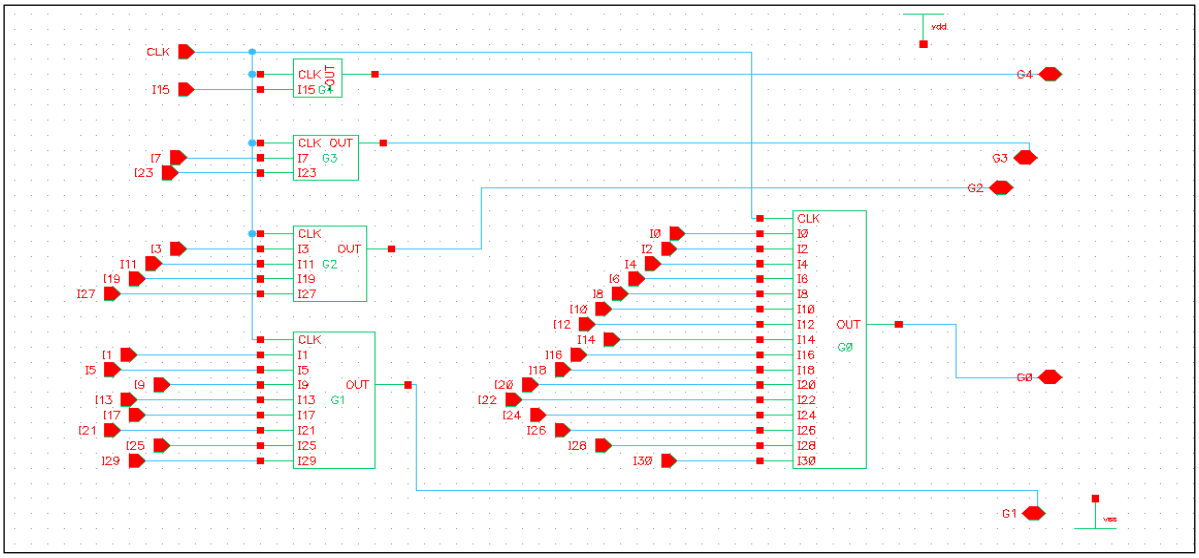

Figure 8. Thermometer code to Gray code conversion

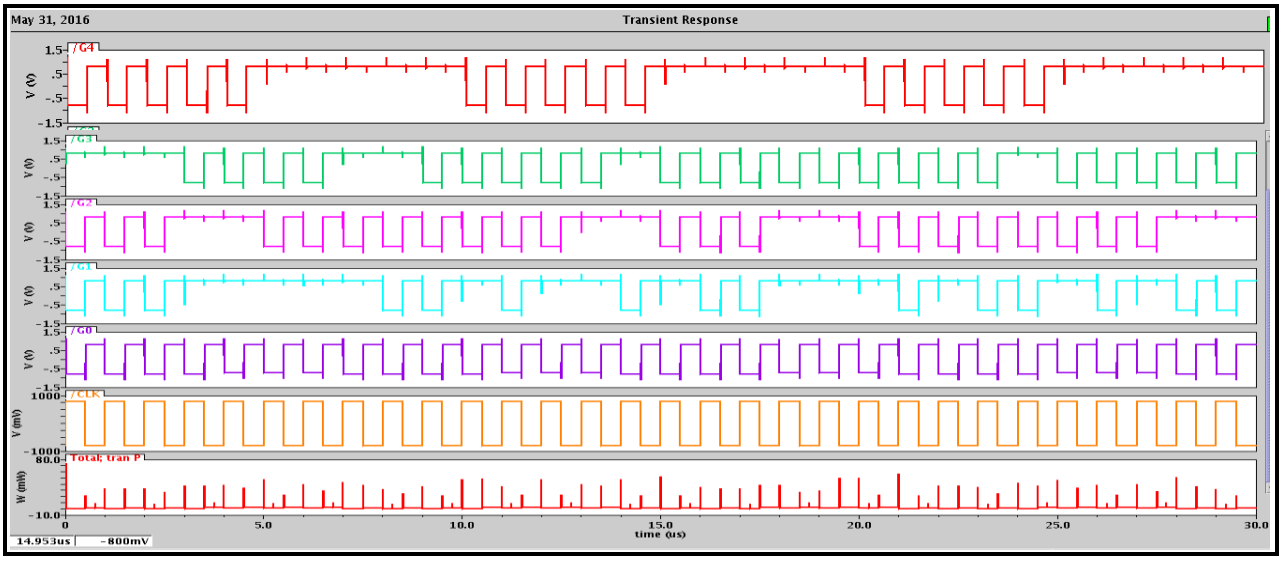

Figure 9. Transient Response of Thermometer to Gray code Conversion

Design of Ex-OR and Ex-NOR circuits is suggested to improve the speed and power of these circuits and is basic building block of many arithmetic circuits [8]. For converting the gray to binary code we are using the Ex-OR gate. The expressions gray to binary conversion are as shown in the below of the table1. This paper Ex-OR gate implemented by adapted merged DCVSL logic. The schematic diagram of Ex-OR gate is as shown in the below figure10. The procedure of Ex-OR gate is if both inputs are same then output will be equal to '0'. If both inputs are

complement to each other inputs then the output will be equal to ‘1’. The adapted merged DCVSL Ex-OR gate has consuming less power and boost the speed of the logic gates.

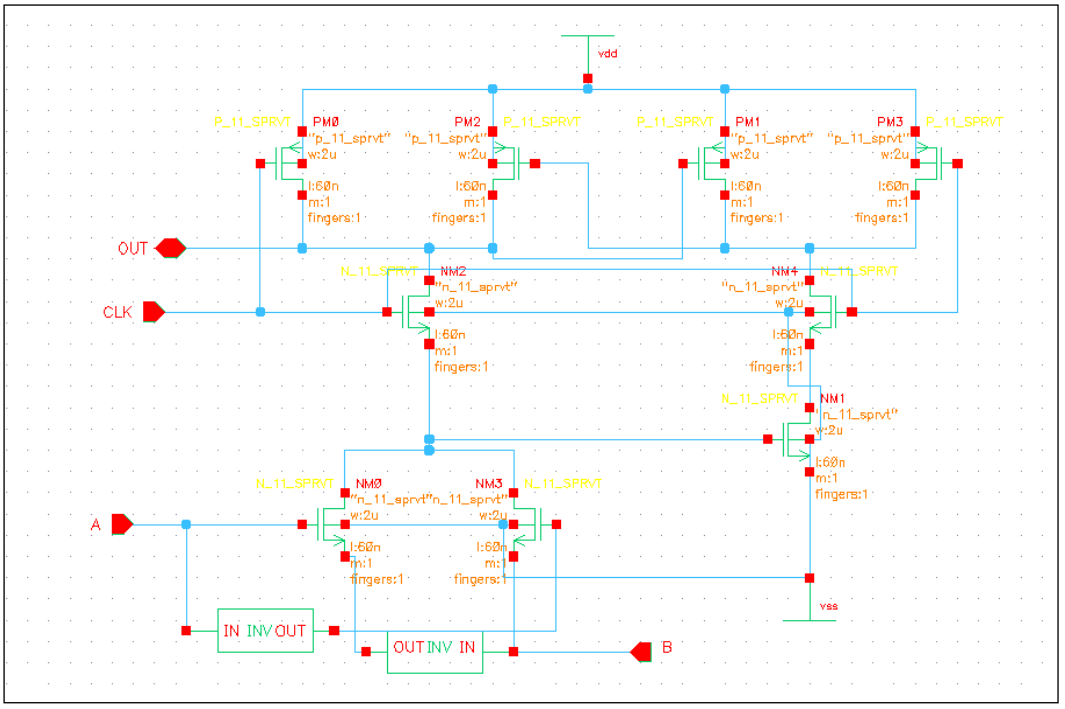

Figure 10. Schematic diagram of Ex-OR Gate

3.2.2 Schematic Diagram of Implemented Flash Analog to Digital Converter

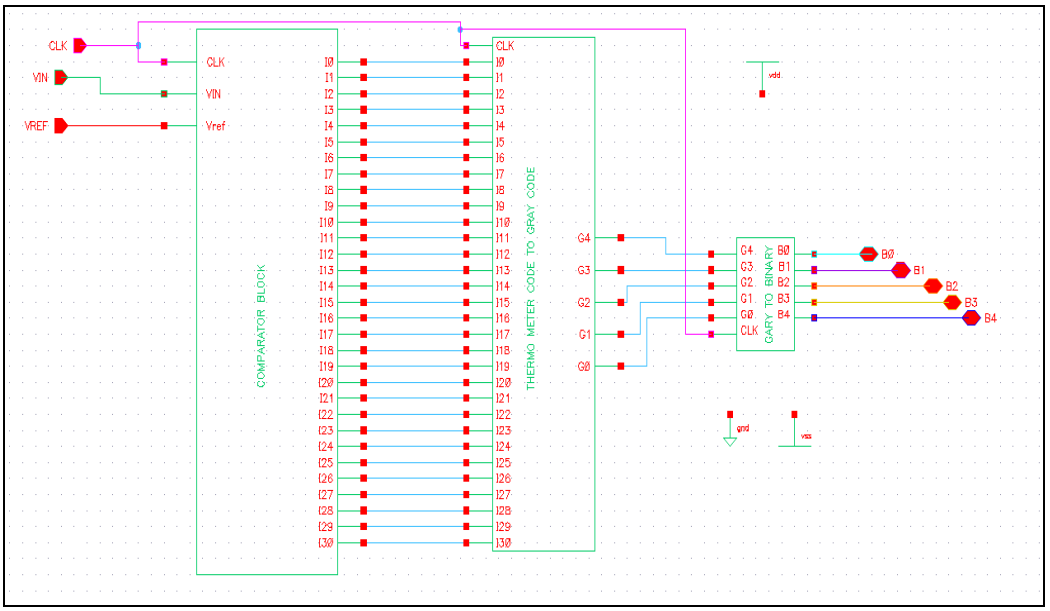

Figure 11. Schematic Diagram of the Implemented Flash Analog to Digital Converter

3.2.3 Transient response of Implemented Flash Analog to Digital converter

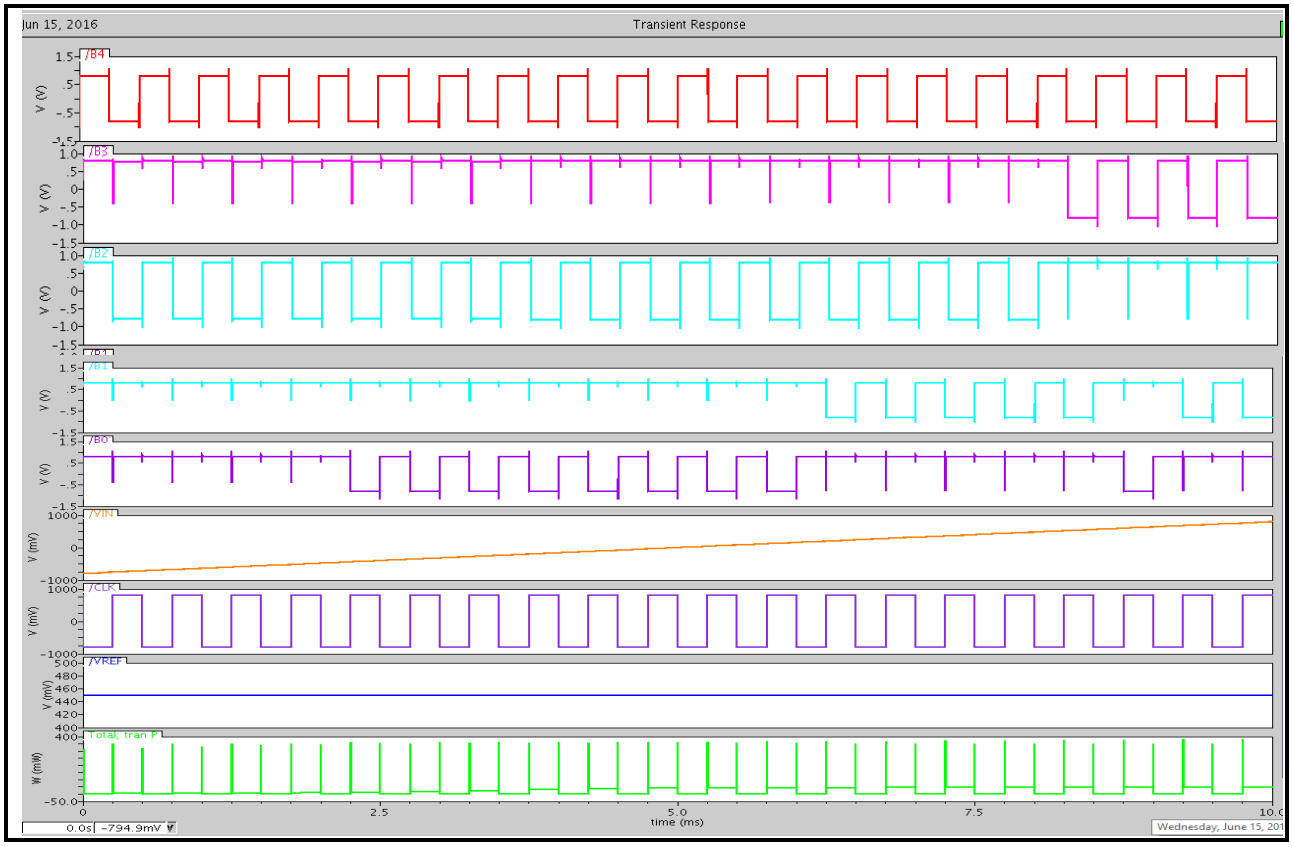

Figure 12. Transient Response of flash analog to digital converter

4. Simulation Results and Discussion

The summary of the results and its comparison table are as shown in the table2.

Table 2. Summary and Comparison of Implemented Flash ADC

	Power & resolution adaptive ADC[9]	2-stage flash folded ADC[7]	DCVSL technique flash ADC[1]	Offset averaging technique ADC[18]	Multiplexer decoder flash ADC[17]	Design and Implemented flash ADC results
Technology (nm)	180	180	180	130	180	65
Resolution	5-bit	5-bit	5-bit	4-bit	5-bit	5-bit
Supply Voltage (V)	1.5	1.8	±0.85	±1	±0.9	±0.8
Analog Input Voltage (V)	-	±0.4	-0.45 to 0.75	1	-0.45 to 0.7	-0.8 to 0.8
Power (mW)	68.63	63	46.69	30	28	16.33
Delay (ps)	-	1.18×10^3	513.25×10^3	-	-	1.542
Power Delay Product (fJ)	-	74.34×10^3	23.96×10^6	-	-	25.18
Sampling Frequency (GHz)	3.03	1	5	1	5	3

5. Conclusion

The implemented schematic diagram of flash ADC and its transient response are as shown in the above figure11 and figure12. The simulated results and comparison of different types of encoding flash ADC [7, 9, 1, 18, 17] is shown in the table2. The input and output combinations of the different bits for 5-bit flash ADC observed on CADENCE tool in UMC 65nm technology. The implemented 5-bit flash ADC achieves the ultra high sampling rate frequencies (GHz). The average power consumption and delay (speed) of the flash ADC is 16.33 mw and 1.542 ps and the power delay product (PDP) or Figure of merit (FOM) of flash ADC is 25.18 fJ. The implemented merged DCVSL based flash ADC reduces power 65.02% compared to DCVSL based flash ADC.

6. References

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