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# Design of MIMO K-Best Detection Algorithm And Its FPGA Implementation<sup>★</sup>

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## Abstract

Based on the research of MIMO Detection Algorithms theory and implementation methods, here novel k-Best MIMO detection algorithm is presented. Proposed algorithm uses an estimate technique and parallel sort approaches, which reduces the computational difficulty, and adopts pipelined configuration in parallel to save computation time. This algorithm implemented on Xilinx virtex-6. Implementation of proposed k-best multiple input multiple output detection algorithm on Field Programmable Gate Array is a challenging task by considering area and power. Computational complexity and resource utilization of this algorithm is discussed by implementing it on Virtex Field Programmable Gate Array. Field Programmable Gate Array implementation attained a good trade-off between power and area compared to the previous designs. Because of pipelined design and sorting procedure it is well suited for FPGA implementation and achieved 2.8 Gbps throughput for 64QAM modulation scheme with 4x4 systems. The flexibility of the scheme permits the high performance detection with low power consumption.

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*Keywords:* MIMO Systems; K-Best; VLSI; FPGA; Circuit Complexity; BER; Sphere Detection.

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## 1 Introduction

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The increasing demand for better data rates and better quality of service in wireless systems have imposed the engineers of the emerging wireless communication systems to develop advanced methods in the direction of enhancements of the spectral efficiency and reliability. Multiple Input Multiple Output (MIMO) technology is one of the approach which offers either greater spectral efficiency [1] or diversity gain. MIMO is used to describe the multiple input multiple output wireless communication system at the transmitter and receiver. One of the main advantages of MIMO is by transmitting number of data streams in parallel among several independent communication channels maximum data rate can be achieved [2]. Therefore MIMO technology is the next generation wireless communication technology because of high data rate, increased system capacity, and the capacity increases linearly as the number of antennas increases. In MIMO detection, sphere detection algorithm is an effective method for which bit error rate performance is close to the optimal ML detection, and also significantly reduces the complexity.

Tree search algorithms balance the performance in accordance with the complexity. In tree search algorithms first one is depth first algorithm in which traversing a tree is in both directions without fixed throughput and because of this hardware implementation is critical. The disadvantage is the search process iterations are more, throughput is less and the complex degree is not fixed, as Schnorr-Euchner Sphere Detection algorithm and List Sphere Detection algorithm. Second algorithm is breadth first search algorithm in which traversing a tree is only in forward direction and throughput is fixed. K-Best method [3] is an approach for breadth first search technique which gives near optimal performance as maximum likelihood detection and better bit error rate because in each cycle parent as well as child nodes are enumerated. If the k value is too high then the computational complexity increases, so to get the optimal performance like ML with reduced complexity k value is to be chosen carefully. K-Best breadth-first algorithm is a popular algorithm because of its feed forward structure, hardware -friendly features in each layer of the detection signal, leaving only the smallest K metric values corresponding to the path to determine the extension which reduces the complexity. On the basis of in-depth research this paper presents k-best sphere detection algorithm based on Prediction and parallel sorting approach, without degradation in performance.

The design tool must be chosen sensibly as the signal processing applications impose substantial limits on area, power dissipation, speed and cost. Digital signal processors (DSPs) and Field programmable gate arrays (FPGAs) are the most generally used tools for the design of such application. The DSPs used for very complex math-intensive tasks but can't process great sampling rate applications due to its architecture. Application Specific Integrated Circuits (ASIC) faces lack of flexibility and requires extensive design cycle. The limitations of DSP and ASIC are overcome by means of single FPGA. Therefore FPGA has become the best choice for the signal processing system designs due to their greater flexibility and more bandwidth, resulting from their parallel architecture [4]. Implementing the design using FPGA is very fast with lower development costs and takes less amount of time. VLSI implementation of the detection algorithms in the MIMO system will turn out to be a crucial approach in the future wireless communication system.

The main theme of this paper is to observe the FPGA implementation which makes the realization of MIMO systems more concrete by improving the performance. Rest of the paper, begins with brief overview of system model in Section 2, and then presented K-Best algorithm in Section 3. Section 4 presents the results of Bit Error Rates (BER) and also hardware implementation results. In Section 5, concludes that the K-Best MIMO receiver effectively used for high speed applications and also the applicability of FPGA system for MIMO detection algorithm in effective and inexpensive way.

## 2. System Model

Consider a MIMO system with  $N_t$  transmitter and  $N_r$  ( $N_r \geq N_t$ ) receiver antennas as shown in figure 1. MIMO input output relationship can be written as

$$y=Hs+n \tag{1}$$

where  $y$  is received signal vector, Transmit Signal vector is  $s$ , and  $n$  is the additive noise vector where each noise component is generally demonstrated as independent identically distributed white Gaussian noise of variance  $\sigma^2$ . In general the transmitted signals are joined in the channel because of same carrier frequency.  $H$  denotes the  $N_r \times N_t$  channel matrix [5] which can be expressed as

$$\mathbf{H} = \begin{pmatrix} \mathbf{h}_{1,1} & \mathbf{h}_{1,2} & \dots & \mathbf{h}_{1,N_r} \\ \mathbf{h}_{2,1} & \mathbf{h}_{2,2} & \dots & \mathbf{h}_{2,N_r} \\ \dots & \dots & \dots & \dots \\ \mathbf{h}_{N_t,1} & \mathbf{h}_{N_t,2} & \dots & \mathbf{h}_{N_t,N_r} \end{pmatrix} \quad (2)$$

In above equation (2) every single  $h_{i,j}$  indicates the attenuation and phase shift between the  $i^{\text{th}}$  receiver and the  $j^{\text{th}}$  transmitter.

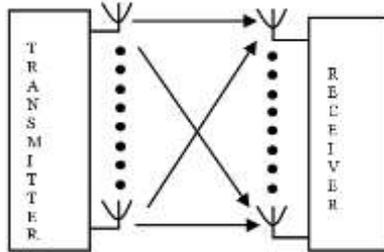


Fig.1. MIMO System Model

At the receiver end, the received signal contains a linear grouping of all transmitted signals plus noise. Then the receiver decides the transmitted signals by considering (1) as a scheme of linear equations. If channel is correlated, the process of linear equations will have increased number of unknowns than the equations. Correlation may occur due to two reasons. To avoid correlation due to spacing between antennas they are generally spaced at least half of the wavelength of the carrier frequency. Another reason correlation may takes place is due to lack of multipath components, so for this purpose rich multipath is required in MIMO systems. The multipath effect can be taken by each receive antenna being in a different channel H.

### 3. ANALYSIS OF ALGORITHMS

#### 3.1 Conventional K-Best algorithm

The Maximum Likelihood (ML) detector equation

$$\mathbf{S}_{ML} = \underset{\mathbf{s} \in \mathcal{A}}{\arg \min} \|\mathbf{y} - \mathbf{H}\mathbf{s}\|^2 \quad (3)$$

By relating QR decomposition on channel matrix H, further it can be written as  $\mathbf{H}=\mathbf{Q}\mathbf{R}$  and

$$\begin{aligned} \hat{\mathbf{y}} &= [\mathbf{y}_1 \quad \dots \quad \mathbf{y}_{N_r-1} \quad \mathbf{y}_{N_r}]^T = \mathbf{Q}^T \mathbf{y} \\ &= \mathbf{Q}^T \mathbf{Q}\mathbf{R}\mathbf{s} + \mathbf{Q}^T \mathbf{n} = \mathbf{R}\mathbf{s} + \mathbf{Q}^T \mathbf{n} \end{aligned} \quad (4)$$

Now maximum likelihood detection formula becomes

$$\mathbf{S}_{ML} = \underset{\mathbf{s} \in \mathcal{Q}^{2N}}{\arg \min} \|\hat{\mathbf{y}} - \mathbf{R}\mathbf{s}\|^2 \quad (5)$$

In K-best breadth first algorithm each and every level of the tree best transmitted symbols are chosen with lowest metric path. The detector output is the path with lowest Partial Euclidean Distance at the last level of tree [6]. When constellation size is increased tree search also grows and it results in increased complexity and to avoid exhaustive search novel techniques are needed.

#### 3.2 Proposed K-Best Algorithm

The advantage of conventional K-Best detection algorithm compared to other sphere detection algorithm is its positive search process by narrowing the search space, and it has a fixed complexity, throughput and is suitable for hardware implementation. At the same time, due to the high complexity of the conventional K-Best algorithm

proposed algorithm focuses on the path cost calculation and sorting operations of each layer. In order to reduce the computational complexity of detection algorithm, novel k-best detection algorithm is introduced. Proposed k-best detector makes use the advantages of the parallel characteristics and fixed throughput of breadth first sphere detection architecture, which outperforms the previously reported algorithms. Its main idea is to improve SE algorithm implementations that is, when determining the extended sub-nodes of each node there is no need to calculate Euclidean distance all the child nodes of each and every node. Above given equation (3) can be considered as K-best sphere detection problem. In general K-best SD searches the tree from the origin to the end nodes by increasing all levels and decides k best symbols with the least metric path in each and every level of the tree. Consider the problem in (2), and let us represent the QR-decomposition of the channel matrix as  $H= QR$ , where Q is a unitary matrix and R is an upper triangular matrix. By applying  $Q^H$  to the (1) results in

$$Z= Q^H y =Rs + V \tag{6}$$

Where  $V=Q^H + n$ . By using the upper triangular matrix nature of R, equation (5) can be further extended which results in tree search problem with twice the number of transmitting antennas levels. To further reduce the computational complexity, an early-pruned technique can be used. That can be described by

$$\hat{s}_i = \frac{\hat{y}_i - \sum_{j=i+1}^{2N_R} R_{ij}s_j}{R_{ii}} \tag{7}$$

Where  $N_R$  number of receiving antennas. There are some approaches which are given below are used to reduce such complexity. First, when k value is greater than the constellation size, when carrying out the path extension for each node, every time it is necessary to completely expand one path at level i and up to constellation paths at level i-1. In this situation, the expansion complexity of any path cannot be reduced. In improved k-best algorithm the key point is to combine prediction algorithm and parallel sorting First, in determining the order in each node expanded child nodes using the above technique greatly reduces the computational prediction child node PED thereby reducing the computational complexity of detection algorithm. Then a parallel sort method is used to conduct sorting operation.

## 4 Results And Discussion

### 4.1 Performance Analysis

Based on the above analysis the extrapolation technique and the parallel sorting K-best algorithm performance is done using MATLAB. Below figure shows the results of MIMO communication using 4x4 and with 64 QAM modulation scheme with K=8, the channel quasi-static flat Rayleigh Fading channel. Below figure 2 shows the performance of proposed K-Best algorithm with conventional K-Best algorithm.

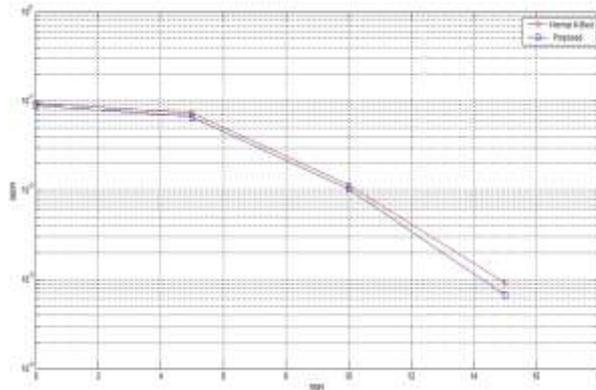


Fig.2 Comparison of Conventional and proposed K-Best algorithms

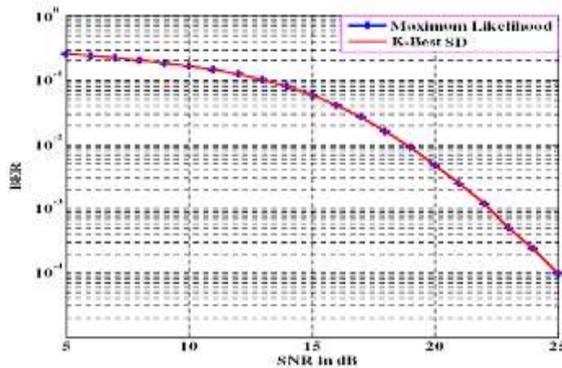


Fig.3 Comparison of ML and proposed K-Best algorithms

This shows that in ensuring the idea of reducing the complexity of the algorithm of the improved K-Best detection algorithm still has a high diversity gain, MIMO communication system to meet the design requirements of a low error rate. Figure 3 shows that the proposed detector performance is same as maximum likelihood detection performance.

#### 4.2 FPGA Implementation

One of the crucial task in the design of K-best VLSI architecture is to attain high speed with minimum number of stages that are being used in the architecture. To solve this issue, a pipelined arrangement is used, which accomplishes the child extension and to reduce to the smallest possible amount in a pipelined approach and then sorting is implemented. The pipelined design includes the sorter stage which resolves all the signals and the Processing Element (PE) stage produces the best signal from the sorted signals. The proposed pipelined VLSI structure for a 64-QAM MIMO detector with 4 x 4 system is shown in Figure4.

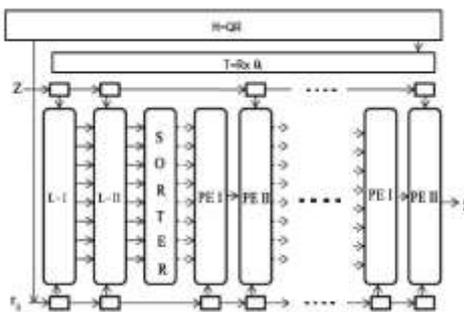


Fig.4 VLSI architecture of proposed K-Best algorithm

The architecture consists two portions and they are processing elements (PE) and Sorter Stage. For handling one survivor node computation circuit is used which computes the percentage of the branch metric and this outcome will be same for the similar parent path. This portion of the execution employs a number of adders and multipliers, and occupies a major amount of area and power consumption. For every node which survives the path metrics can be computed using processing elements and it also detects the active child's for the received symbol. Processing elements run in parallel and each PE operates on one candidate to reduce the time. Thus, each stage requires only a PE detection unit structure, in terms of the system, the total number of PE units is 8.

Here the system model is for 4 transmitting antennas so the design consists of twice the transmitting antenna levels that are 8 levels from level 1 to level 8. K-best detection algorithm calculates the lowest PED. According to the features of the algorithm, to achieve the high speed requirements, to save processing time pipelining and parallel processing is used in the design. The pipeline architecture allows data processing in each clock cycle, at each level of the detection signal, leaving only the smallest K metric values corresponding to extend the path to determine the

situation. Sorter stage first sort all the first child's then from it the first child with lowest PED is calculated. Sorter stage takes four cycles to sort eight PEDs. By using this approach the number of clock cycles required for sorting is less compared with other sorting techniques. In each and every level one PE-I and one PE-II blocks are there to produce k-best list of the present level and to produce and sort the all first child's of the present level.

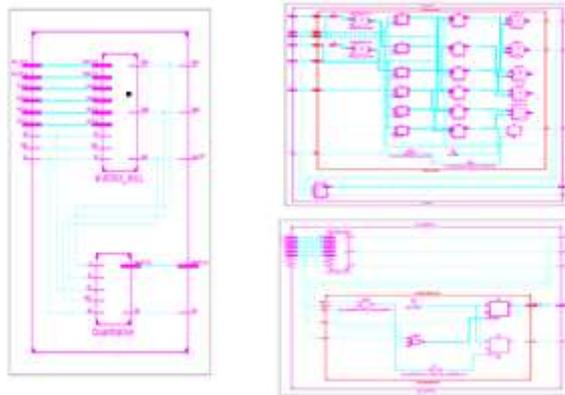


Fig.5 RTL Schematic of K-Best Sphere Detector

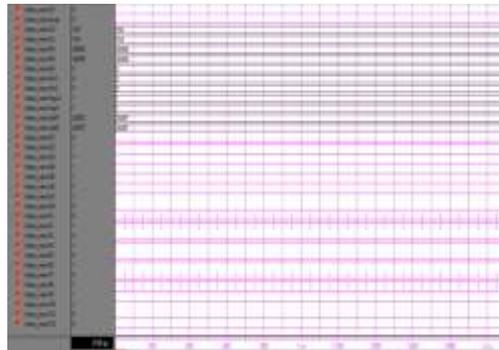


Fig. 6 Simulation Results of of K-Best Sphere Detector

Table 1. Device Utilization Summary.

**Device utilization summary for Proposed Detector**

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**Selected Device : Virtex 6- XC6VLX75TFF484-3**

**Slice Logic Utilization:**

Number of Slice Registers	: 152 out of 4800	3%
Number of Slice LUTs	: 510 out of 2400	21%
Number used as Logic	: 510 out of 2400	21%

**Slice Logic Distribution:**

Number of LUT Flip Flop pairs used	: 543	
Number with an unused Flip Flop	: 391 out of 543	72%
Number with an unused LUT	: 33 out of 543	6%
Number of fully used LUT-FF pairs	: 119 out of 543	21%
Number of unique control sets	: 9	

**IO Utilization:**

Number of Ios	: 57	
Number of bonded IOBs	: 57 out of 102	55%
IOB Flip Flops/Latches	: 1	

**Specific Feature Utilization:**

Number of BUFG/BUFGCTRLs	: 1 out of 16	6%
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Figure 5 and 6 shows the schematic and simulation results of proposed k-best detector. The design was developed using Hardware Description Language and synthesized to Xilinx Virtex 6 FPGAs. Fig.7 is about device utilization

summary for proposed K-Best detection algorithm. The synthesis results show that the design is capable to achieve processing at faster rates and achieves the real-time requirements. The structural design is consuming less resource when compared with other related works.

## 6. Conclusions

Through this approach, the architectural implementation of proposed K-best algorithm reduces the computational hardware complexity of multipliers in conventional design. The parallel execution decreases the number of nodes visited in the process. Hence, the total number of clock cycles necessary to compute the PEDs is also reduced. The sorting difficulty is also reduced in proposed strategy which leads to efficient implementation. The proposed method can be extended for higher order modulation with different antenna configurations for high speed applications with low power requirements.

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