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Xilinx Spartan 3A DSP FPGA based DC Voltage Regulators for PV Systems

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Abstract

This paper explains the design and implementation of Perturb and Observe Maximum Power Point Tracking Algorithm combined with the Closed Loop Digital PI control algorithm to generate the Digital Pulse Width Modulation using Xilinx Spartan 3A DSP Field Programmable Gate Array for regulating the load voltage of DC-DC buck converter. And also concentrates on the methods for generation of DPWM techniques say Delay line based Digital Pulse Width Modulation and Hybrid based Digital Pulse Width Modulation with the 2^{10} bit resolution. All the algorithms are developed by VHSIC Hardware Description Language coding and are implemented using Xilinx ISE 12.1 tool. The hardware results validate the satisfactory voltage regulation of PV system under continuous changing weather condition. The Hybrid based Digital Pulse Width Modulation seems to have better time transient response than the Delay line based Digital Pulse Width Modulation.

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Keywords: Field Programmable Gate Array , Perturb and Observe Algorithm, Maximum Power Point Tracking, Digital PI Control, Digital Pulse Width Modulation Techniques, DC-DC Buck Converter.

1. Introduction

The Solar Energy is the most effective and efficient renewable source. The PV cell is a component which is similar to PN junction diode except that the PV cell operation is based on the Sun's irradiation. The PV cell has many advantages like low maintenance cost, less power loss and reliable energy source. This paper concentrates on the FPGA implementation of the P & O MPPT algorithm and the closed loop DPI controller for load voltage regulation of the DC-DC buck converter in real time using Xilinx Spartan 3A DSP FPGA.

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FPGA device has many advantages like parallel processing, designing is easy, high speed of operation and consumes low power. The P & O MPPT algorithm is considered for controlling the DC-DC buck converter. Without the use PV parameters, the MPPT is implemented using FPGA [1]. The Perturb and Observe Algorithm is implemented using FPGA for the tracking of MPP has low cost [2]. Digital FPGA Controlled DC-DC Buck Converter provides smooth and stable regulated output voltage [3]. The FPGA model of DC-DC buck Converter increases operational safety, resulting in substantial power converter and reduces cost [4] [5]. The PID controlled DC-DC buck converter is easy to design and implemented in FPGA [6].The FPGA based DPWM control is very simple and reliable [7]. FPGA based DPWM requires less complexity in design [8]. In this paper, the real time FPGA implementation of P&O MPPT algorithm is discussed first and closed loop DPI controller algorithm for DC-DC Buck Converter is explained in the next section.

Nomenclature

ADC	Analog to Digital Converter
CDPWM	Counter based Digital Pulse Width Modulation
DC	Direct Current
DCVM	Direct Current Value Match
DDPWM	Delay line based Digital Pulse Width Modulation
DPI	Digital Proportional Integral
DPWM	Digital Pulse Width Modulation
DSP	Digital Signal Processing
FPGA	Field Programmable Gate Array
HDPWM	Hybrid based Digital Pulse Width Modulation
MPP	Maximum Power Point
MPPT	Maximum Power Point Tracking
P&O	Perturb and Observe
PID	Proportional Integral Derivative
PV	Photo Voltaic
SCC	Signal Conditioning Circuit
VHDL	VHSIC Hardware Description Language
VHSIC	Very High Speed Integrated Circuit
ZVM	Zero Value Match
V_{PV}	PV Voltage
I_{PV}	PV Current
V_{VPV}	Signal conditioned PV Voltage
V_{IPV}	Signal conditioned PV Current
V_{LOAD}	Load Voltage
Δd_1	Duty Cycle from the MPPT Algorithm
Δd_2	Duty Cycle from the Closed Loop DPI Controller Algorithm
Δd_T	Total Duty Cycle($\Delta d_{1+} \Delta d_2$)
ΔP	Difference in Power
ΔV	Difference in Voltage
t_d	Delay Time
t_p	Peak Time
t_r	Rise Time
t_s	Settling Time
ess	Steady State Error
%MP	Percentage Peak Overshoot

2. Maximum Power Point Tracking

2.1. Perturb and Observe Algorithm

The MPPT algorithm is responsible for the PV modules to always operate at its maximum power. There are different MPPT techniques and in this paper P&O algorithm is used to track the maximum power. It is an online technique and mostly preferred for its simplicity and easy implementation. Direct duty ratio P&O method is used here in which D is taken as the control parameter. The principle of the P&O algorithm is to sense the PV output voltage (V_{PV}) and output current (I_{PV}) and calculate the power. The P&O algorithm utilizes the Voltage and Power for the updating of the Maximum Power Point (MPP). For every value change in the V_{PV} & I_{PV}, the value of Power ($P=V_{PV} \times I_{PV}$) is calculated and updated accordingly.

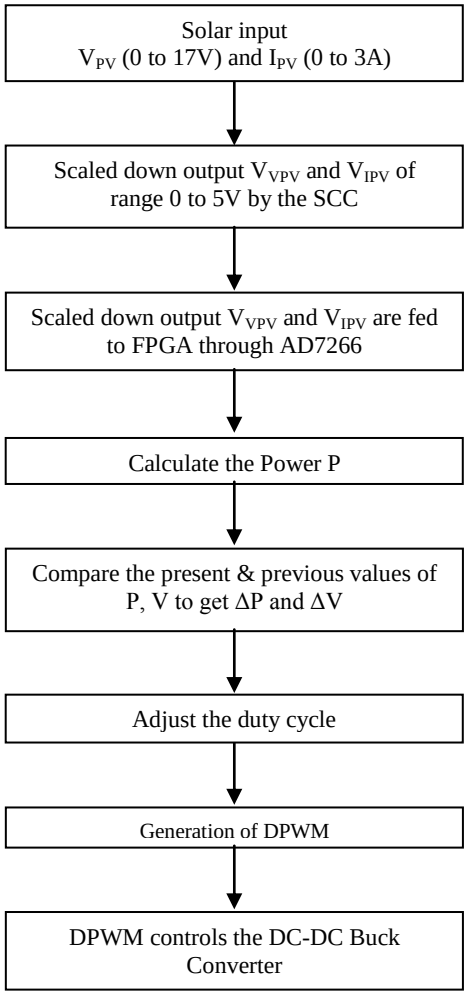


Fig.1 Design flow for the P&O MPPT algorithm using FPGA

Figure.1 depicts the design flow of P&O algorithm using Xilinx Spartan 3A DSP FPGA. For real time FPGA implementation the solar voltage range from 0 to 20V is attenuated by the Signal Conditioning Circuit (SCC) to 0 to 5V.Current is also sensed in terms of voltage of the same range. The solar voltage and current thus sensed are fed as solar inputs to the FPGA Spartan 3A DSP to calculate the power and compare with the previous power and voltage to get ΔP and ΔV. ΔP and ΔV are compared with zero and if positive then the operating point is at the left of the MPP and the duty cycle of the converter is decreased and if negative its vice versa. The increase and decrease of the

duty cycle by a constant step size tracks the MPP. Selection of step size plays a vital role in the rate of MPP tracking.

2.2. Digital Pulse Width Modulation Generation

The Digital Pulse Width Modulation (DPWM) techniques are classified into three types. They are

i. Counter based DPWM (CDPWM),
ii. Delayline based DPWM (DDPWM) and
iii. Hybrid based DPWM (HDPWM).

i. Counter based DPWM

In counter based DPWM generation method, an asymmetric carrier wave is generated by the counter. The counter based DPWM method can be designed in three ways depending on the triggering direction of the counter circuit. If the direction of the counter is in increasing value (UP COUNTER), then it is called as leading edge counter based DPWM. If the direction of the counter is in decreasing order (DOWN COUNTER), then it is called as trailing edge counter based DPWM. If the direction of the counter is increasing and decreasing (UP/DOWN COUNTER), then it is called as triangular counter based DPWM. Switching period value is equivalent to the highest count value. The block diagram of the counter based DPWM is given in figure 2.

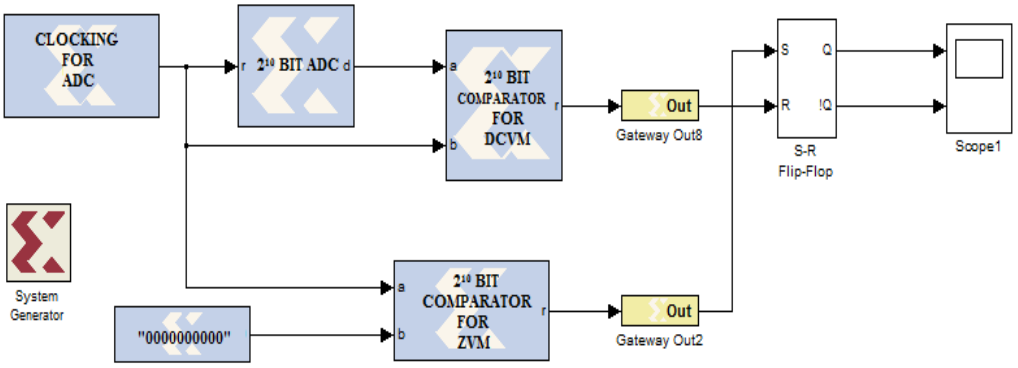


Fig. 2 SIMULINK-MATLAB model for CDPWM

The first comparator block finds the initial value match (namely zero "0") of the counter. This is referred as "Zero Value Match" (ZVM). The second comparator block finds the match value between the counter and the digitized DC input value. This is referred as "DC Value Match" (DCVM).The ZVM is the input to the SET and DCVM is the input to the RESET of the SR-flip flop. The SR-flip flop is triggered by these two signals namely SET and RESET to generate the DPWM.

ii. Delay line based DPWM

Figure 3 shows the SIMULINK-Xilinx block set for the 10-bit resolution Delay line based DPWM method. Delay line based DPWM generation method involves the 2^{10} ring counter, 1024:1 multiplexer and SR-flip flop. The converted 10-bit Duty value is fed as select line for the 1024:1 multiplexer. 2^{10} ring counter is connected to the input side of the 1024:1 multiplexer through 1024 D-flip flops as shown in figure 4. The SET signal of SR-flip flop is enabled by the 1023rd pin of the ring counter through its corresponding D-flip flop. The RESET signal of SR-flip flop is enabled by the 1024:1 multiplexer output. Thus the DPWM is generated by the SR-flip flop to operate the DC-DC buck converter.

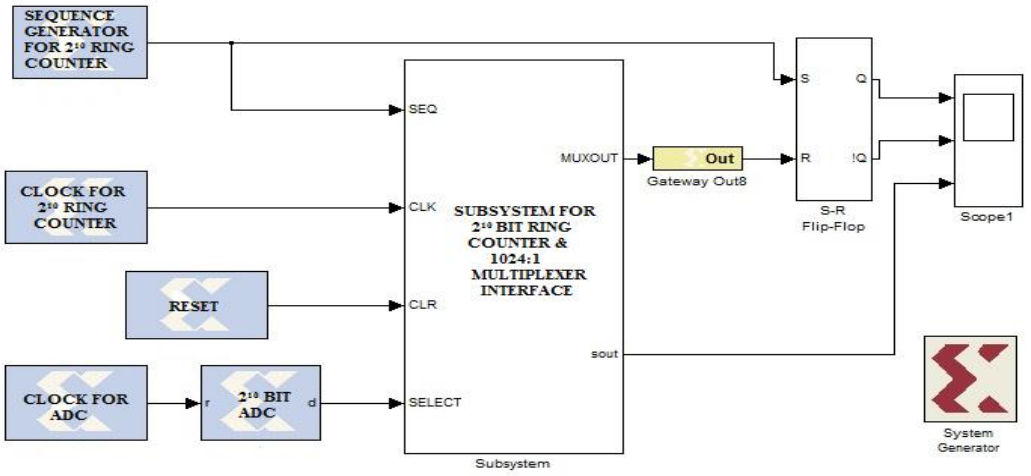


Fig. 3 SIMULINK-MATLAB blockset model of Delay line based DPWM

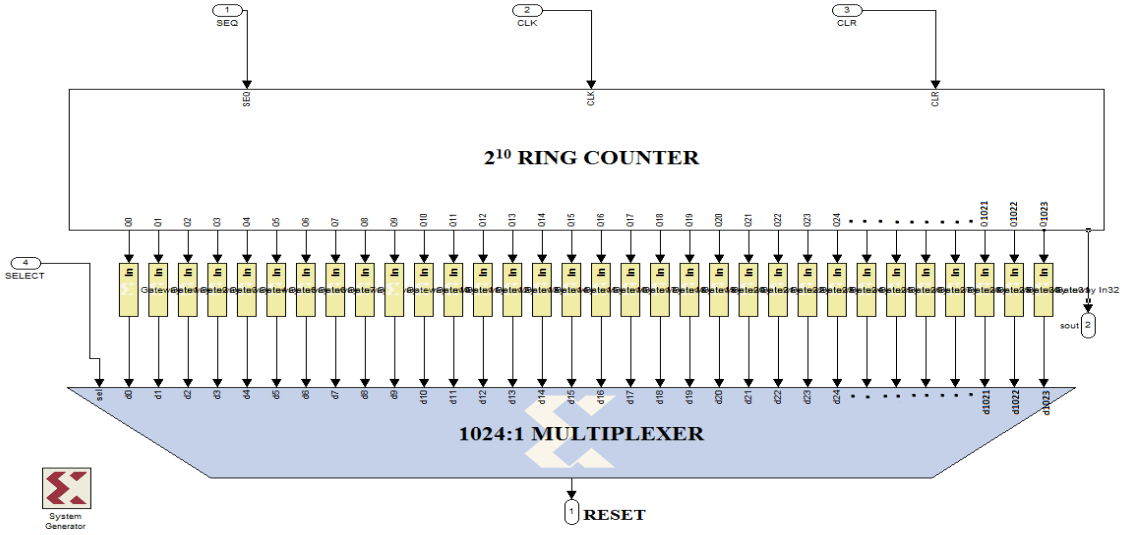


Fig.4 SIMULINK-MATLAB blockset for 2^{10} Ring Counter and 1024:1 Multiplexer Subsystem

iii. Hybrid based DPWM

Hybrid based DPWM generation method is the combination of both counter based DPWM and delay based DPWM methods. The DC input signal of 10-bit resolution is bit split into 2^5-bit and 2^5-bit resolutions. In which 2^5-bit resolution is used for the generation of the Delay line based DPWM generation and 2^5-bit resolution for the generation of the counter based DPWM generation. The hybrid has two SETs and RESETs signals(each from counter based and delay line based DPWM generations).These two SET signals are logically AND for the set input and two RESET signals are logically AND for the reset input of the SR-flipflop as shown in figure 5.

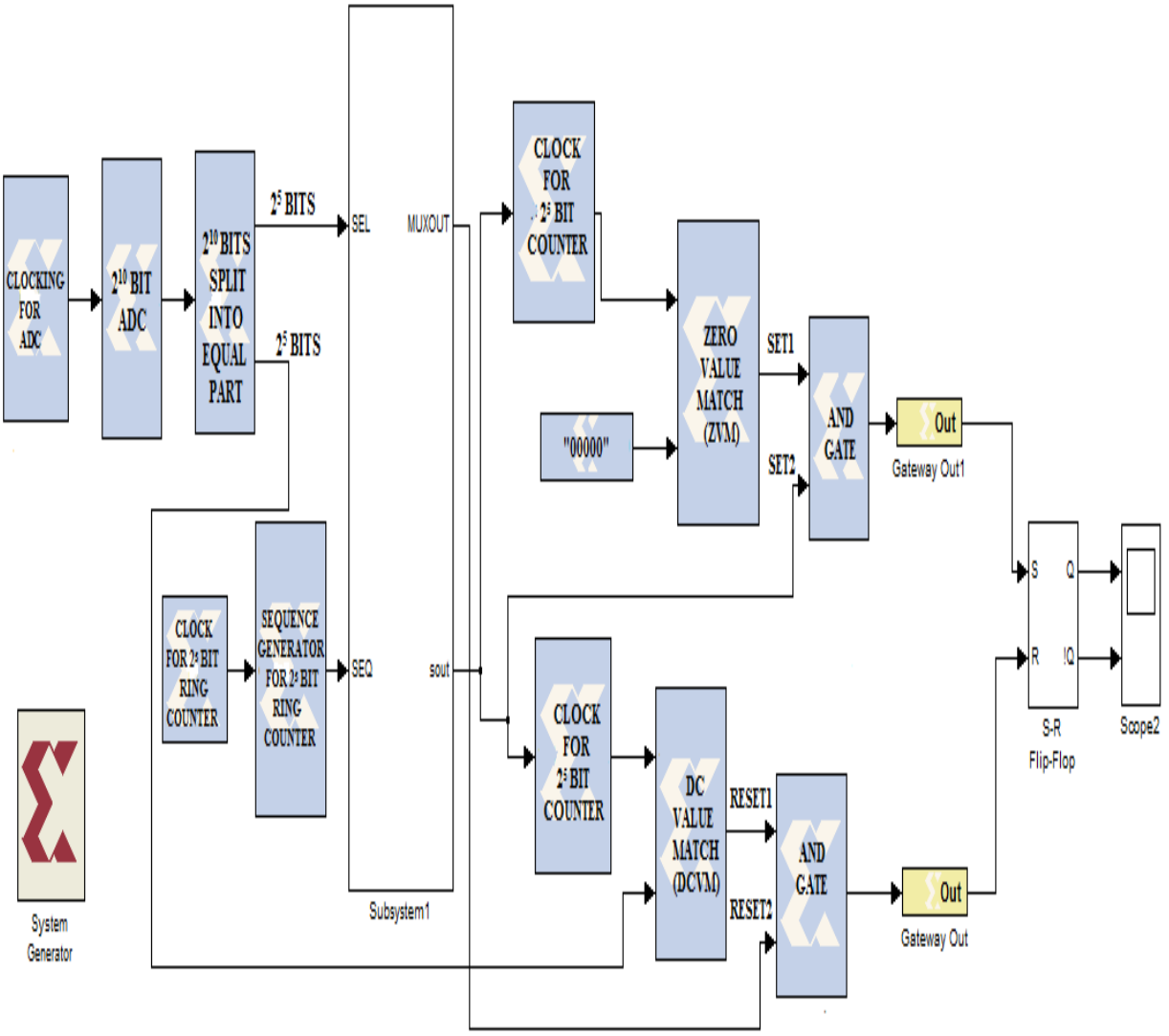


Fig 5. SIMULINK-MATLAB blockset model for Hybrid based Digital Pulse Width Modulation

2.3 Closed Loop PI controller algorithm for DC-DC Buck Converter

The feedback value is taken into the FPGA through the ADC AD7266 so as to compare the actual value with the reference value by using Digital PI controller. The VHDL code for PI controller stabilizes the DC-DC buck converter. The values of K_P and K_I are tuned using Zeigler Nicholas Method. The DPI controlled value is converted to 2^{10} bit equivalent to select the step size. The design flow of the closed loop DPI controller using HDPWM is shown in figure.6

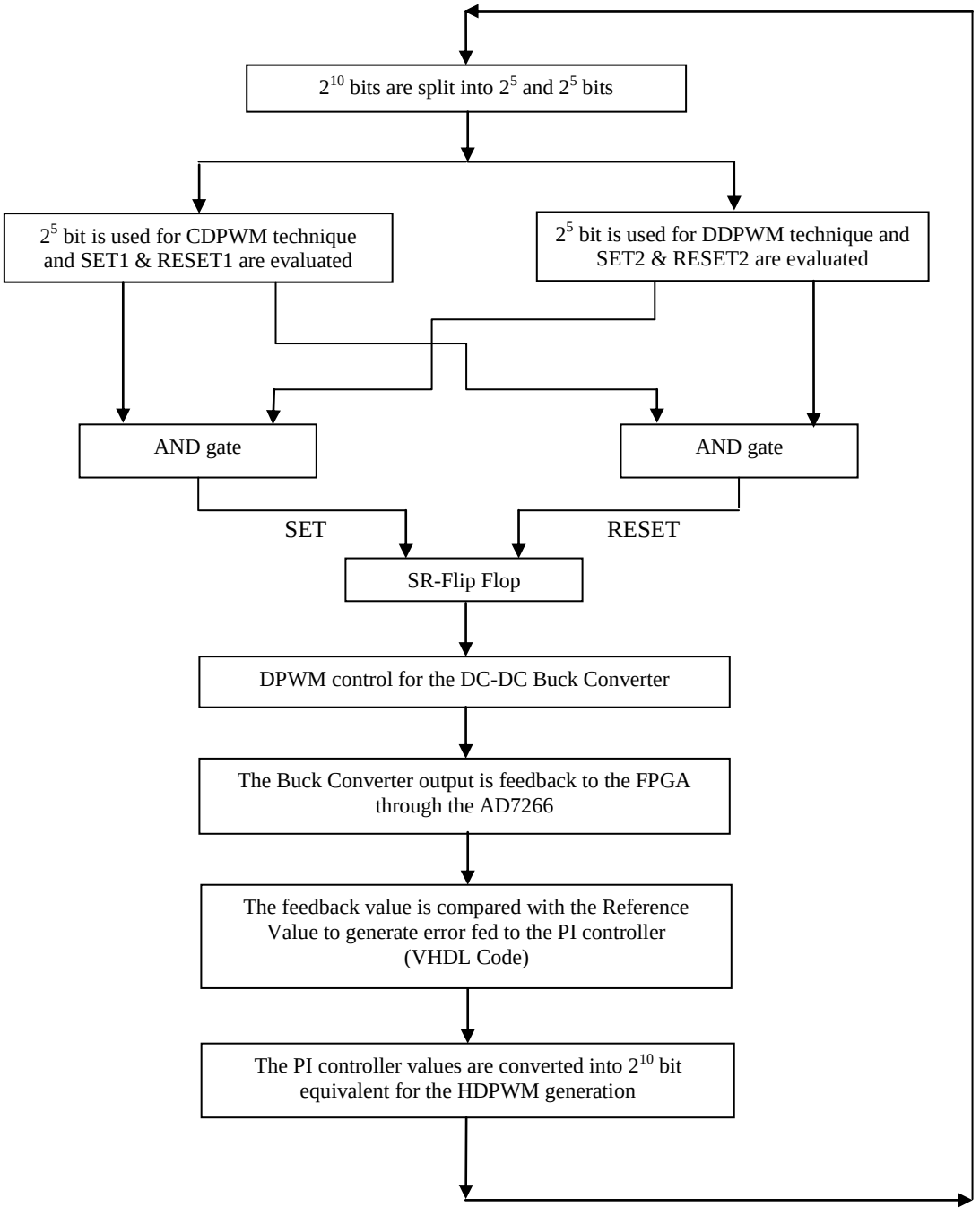


Fig.6 Design Flow for the closed loop DPI control DC-DC buck converter using Hybrid DPWM

3. The Proposed Method

3. MPPT combined with Closed Loop PI controlled DC-DC Buck Converter

The proposed method is combining the MPPT algorithm with the closed loop PI controller. The values of V_{PV} & I_{PV} are scaled down to the range 0 to 5V in order to suit the FPGA device. The scaled downed values of V_{VPV} & V_{IPV} from the SCC are given to the 2 channels of the ADC in the FPGA. The FPGA device manipulates the Maximum Power Point and generates the duty cycle Δd_1 in 2^{10} bit resolution. Concurrently the FPGA does the processing for the closed loop DPI controller algorithm which generates the second duty cycle Δd_2 in 2^{10} bit resolution. The changes in duty cycles Δd_1 and Δd_2 are added with the bias to get total duty (Δd_T). The total duty (Δd_T) is utilized for the generation of Digital Pulse Width Modulation. Figure 7 shows the block diagram of the proposed method.

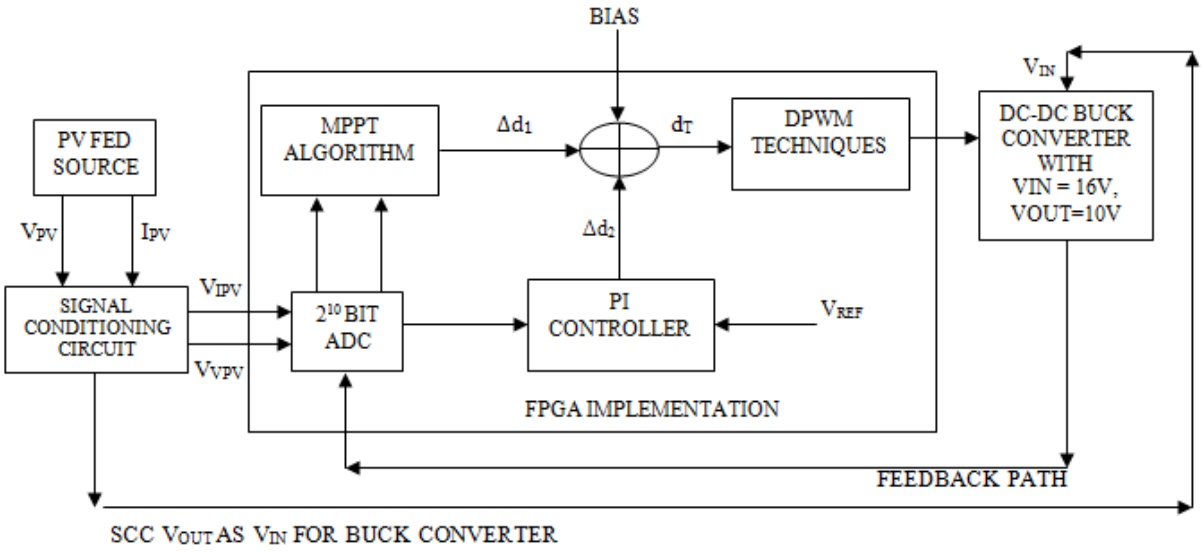


Figure 7. Proposed Method with P&O MPPT algorithm with the closed loop PI controller for DC-DC buck converter

The SCC provides the bridge between the real time values and the FPGA device. The voltage and current from the PV module is fed into the signal conditioning circuit. The signal conditioning circuit converts the voltage of 0 to 20V equivalent to 0 to 5V and current of 0 to 3A as 0 to 5V. The current is measured in terms of voltage. This is performed to make the V and I values suitable for FPGA inputs. The SCC is designed using a Hall Effect Sensor for the Current and Operational Amplifier TL084 for the Voltage. The FPGA has 8 channels ADC (AD7266) with maximum value of 5V for each channel. For this algorithm, the FPGA utilizes three channels concurrently. The V_{VPV} and V_{IPV} are fed through the two channels of the ADC and one channel for the closed loop DPI controller. The values of V_{VPV} and V_{IPV} are converted to 2^n bit equivalent within the VHDL code.

4. Results and Discussion

Figure 8 & 9(a) show the start-up transient response and the steady state response of the P&O MPPT algorithm with the closed loop DPI controller algorithm for DDPWM based DC-DC buck converter. The time transient parameters like ts, tr, td, tp, ess and %MP are evaluated. The set point is 10V and input voltage of the buck converter varies between 13V to 17V. The start up transient for V_{VPV}, V_{IPV} and V_{LOAD} are shown in the Figure 9(b).
Figure 10 & 11(a) show the improved time transient parameters for the P&O MPPT algorithm with the closed loop DPI controller for HDPWM based DC-DC buck converter. The settling time for the HDPWM is better than DDPWM method. The set point is 10V and the input varies from 13V to 17V. The start up transient for V_{VPV}, V_{IPV} and V_{LOAD} are shown in the Figure 11(b). The experimental setup for the above technique is shown in Figure 13. The Table 1 proves the improvement of the HDPWM method in comparison with DDPWM with respect to the start

up time transient response and steady state response. Table II shows device utilization chart for the two techniques and clearly shows that the HDPWM occupies less area and consumes low power.

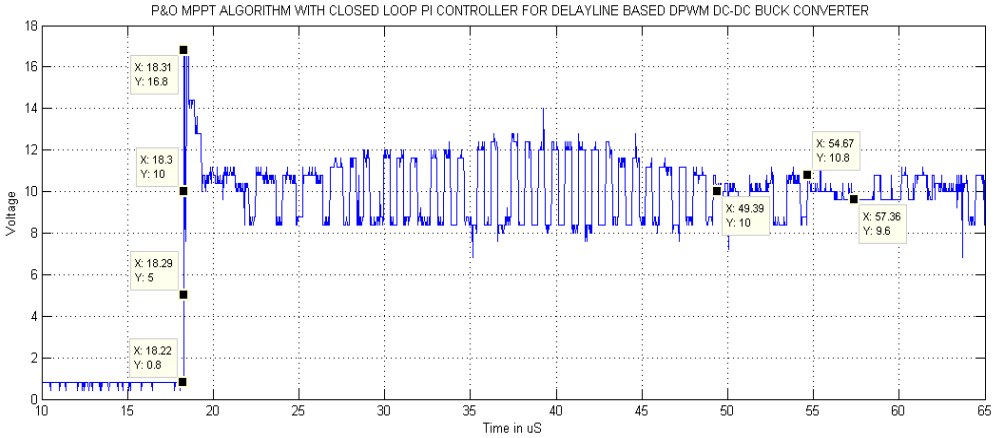
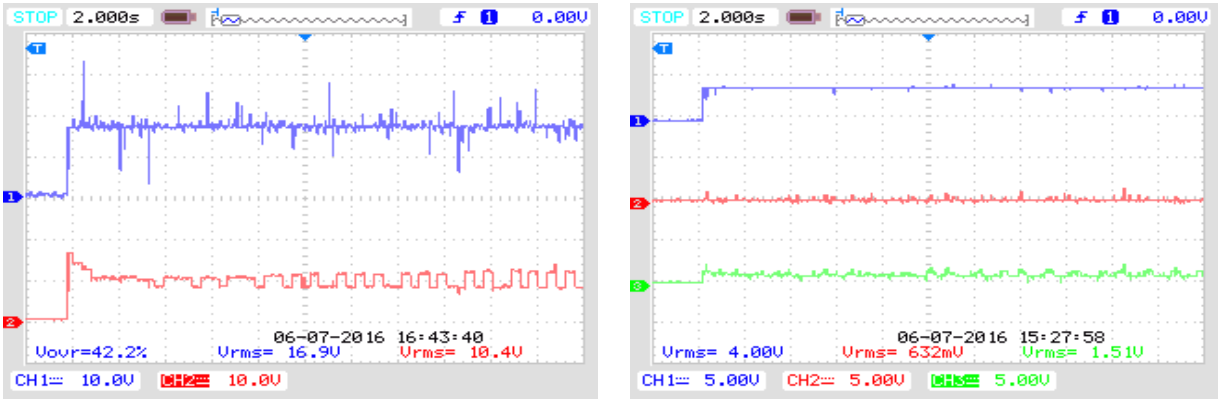


Figure 8 Start up Transient Response of P&O MPPT algorithm and Closed Loop DPI controlled DC-DC Buck Converter using DDPWM imported from CSV.



(a) (b)

Figure 9(a).Experimental result for the V_{PV} in the P&O MPPT algorithm and Closed Loop DPI controlled DC-DC Buck Converter using DDPWM technique; (b) Experimental result for the V_{VPV}, V_{IPV} and V_{load} for the P&O MPPT combined with Closed Loop DPI controlled DC-DC Buck Converter using DDPWM technique.

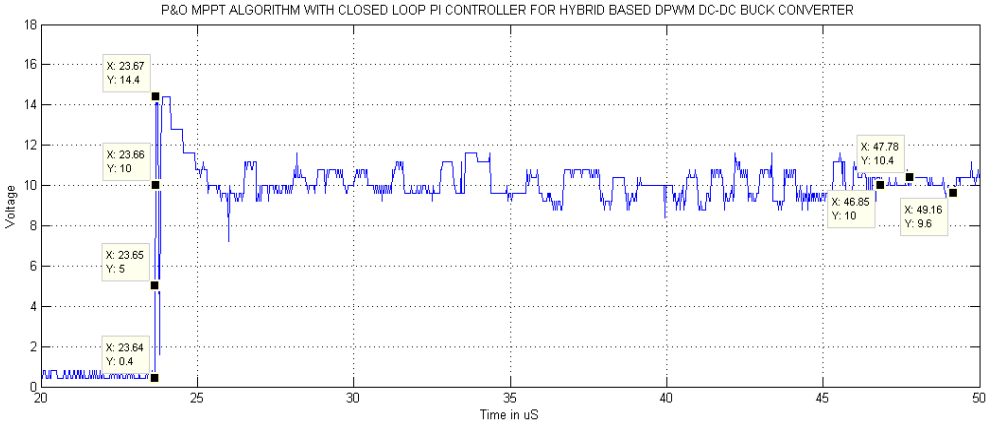


Figure 10. Start up Transient Response of P&O MPPT algorithm and Closed Loop DPI controlled DC-DC Buck Converter using HDPWM imported from CSV.

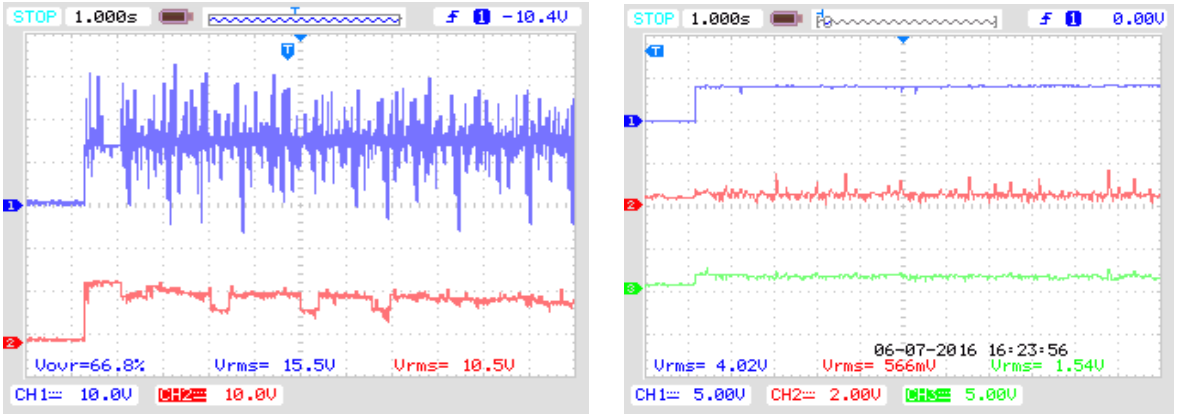


Figure 11.(a) Experimental result for the V_{PV} in the P&O MPPT algorithm and Closed Loop DPI controlled DC-DC Buck Converter using HDPWM technique; (b). Experimental result for the V_{VPV}, V_{IPV} and V_{load} for the P&O MPPT combined with Closed Loop DPI controlled DC-DC Buck Converter using HDPWM technique

Fig 12. Experimental Setup for the proposed method

Table 1. Start-up Transient with the Timing parameters for DPWM Techniques for the proposed method

Method	Delay Line based DPWM	Hybrid based DPWM
Settling Time in μs (**t_s**)	31.11	23.21
Rise Time in μs (**t_r**)	0.08	0.02
Delay Time in μs (**t_d**)	0.07	0.01
Peak Time in μs (**t_p**)	0.06	0.03
Steady State Error (**e_{ss}**)	0.1111	0.0769
Percentage Overshoot (**%MP**)	68%	44%
Set point value (**SP**)	10 V	10 V

Table 2. Device Utilization Chart for DPWM Techniques for the proposed method

Methods	Delay Line based DPWM	Hybrid based DPWM
Resolution with specification	2^{10} 1024 : 1 Mux Designed	$2^{10}=2^5+2^5$ 5-bit Counter & 32:1 Mux Designed
Number of Sliced Flip Flops	2356	1362
Number of 4 input LUTs	3055	2572
Number of occupied slices	3098	1858
Number of bonded IOBs	45	45
Average Fan-out of Non-clock nets	2.65	2.66

5. Conclusion

This paper proves that the start up transient response and steady state response for the real time Xilinx Spartan 3A DSP FPGA implementation of Hybrid based Digital Pulse Width Modulation technique for the PV fed P&O MPPT algorithm and closed loop DPI controller algorithm for the DC-DC buck converter is satisfactory. The area occupancy, power consumption and cost of the HDPWM is very much reduced in comparison with the Delayline based DPWM technique based algorithm. Future works could be directed towards interconnecting of the proposed method with the Multi-Level Inverters.

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