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LOW POWER SCHMITT TRIGGER BASED SRAM USING 32NM FINFET DEVICES

Manish Shrivastava[a], Vimal Kishore Yadav[a*]

[a]*Department of Electronics and Communication, Amity university ,Gwalior (M.P.),474001,India*

Abstract

In this work we propose a novel Schmitt Trigger FinFET SRAM cell. The proposed SRAM cell is focused on high noise immunity and low static leakage, the cell uses two modified Schmitt Trigger based inverters in cross coupled manner. Use of Schmitt Trigger in place of inverters improves noise margin and read performance of the cell. The proposed cell uses FinFET devices in shorted gate and independent gate modes, helping in achieving low static leakage. The proposed SRAM cell shows considerable improvement in performance in terms of SNM, static power consumption and read/write delays due to its modified structure.

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Keywords: Schmitt Trigger SRAM, FinFET, SNM, SPICE;

1. Introduction

According to Moore's law [4], thousand of transistor's can be implemented on a single chip and their numbers are doubled by passing every one and half year. In the present scenario memory allocation and storage problem is there in the field of technical field. Actually this problem occurs because of the memory power consumption, leakage and cost. For reducing these problems so many technologies is worked and FinFET is also the one technology to do this which is literally very useful to reduced that cons. Many types of SRAM is already there in the market like, Architecture of 8T SRAM cell [5] is made up by FinFET features which is independent front and back gate. When controlling the back gate of cell low power consumption SRAM is made. And in 6T SRAM cell architecture [6] two

* Corresponding author. Tel.: +91 9407472058; *.E-mail address:* ervimalyadav@gmail.com

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known gating techniques is used which are incorporating fine grain and coarse grain for calculating the static noise margin, delay, and power of the cell.

2. Static Memory: In a static memory circuit the data stored cannot be changed or deleted until the power supply is connected even if we refreshed it by any other internal or external source the data remains same into static memory circuit, It is because in its data storage cell (1-bit memory cell) in static RAM consists of a simple latch circuit with two stable operating points. As per the state of the two inverter latch circuit the data held being interpreted as either logic "0" or logic "1" , which can be accessed by a bit line for this at least one switch is required which is controlled by the word line. There were some drawbacks occurred in static RAM which are like leakage current, power consumption, stability etc. which can be demolished by using FinFET technology. In this research we have discussed on some static RAM which are based on Schmitt trigger circuit.

3. FinFET: Fin Shaped Field Effect Transistor

According to [2] FinFET technology a kind of multigate or trigate architecture is the key part of smaller and efficient microprocessors and memory cells, which are helpful in increasing the power consumption and performance. FinFET is used to reduce the leakage currents and because of that high leakage current problem is overcome. FinFET technology is generally used to reduce the short channel effects (SCE) and leakage currents. Earlier MOSFET is used for covering up this type of issues but FinFET is best among them and is highly useful to reduce this phenomenon. Threshold voltage can also be controlled with FinFET using metal gate work function. By shorting the two gates of FinFET high performance can be achieved and by controlling these two gates independently leakage would be reduced. They are also helpful in reducing number of transistors by which design space gets reduced. It is easy to deploy it with conventional CMOS to manufacture due to FinFET Compatibility with CMOS shows the multi FinFET [3]. It is made up of a thin silicon body, whose thickness is denoted by TSI, covers by gate electrodes. The channel formed perpendicular to the plane of the wafer, whereas current flows parallel to the wafer plane [3]. Hence it is also known as quasi-planar. Working of FinFET is based on three types of modes which are:

i. Shorted Gate Mode: When both the gates connected together.
ii. Independent gate mode: Gates are controlled independently.
iii. Low power mode: one gate is connects to reverse bias to reduce leakage. It reduces the leakage current as compared to the shorted gate mode.

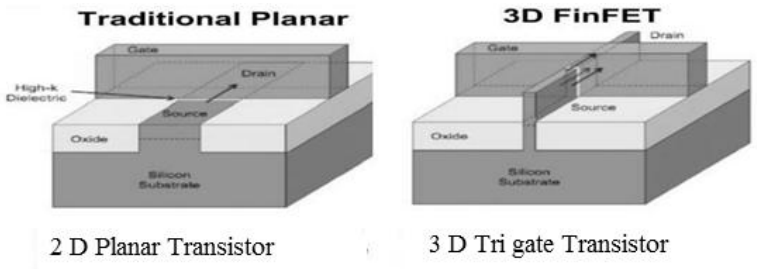

Fig 1: Structure of FinFET

4. Proposed Technique:

Proposed cell uses two cross coupled Schmitt Trigger based inverters. The modified Schmitt trigger is shown in Figure below.

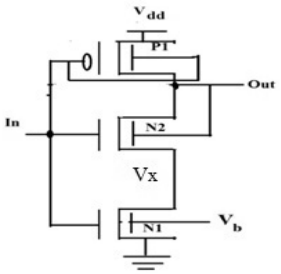

Fig: 2 Modified Schmitt Trigger

The design of Schmitt trigger shown above eliminates need of extra transistor to pull up potential of node Vx [1]. Modified design uses N2 in independent gate mode to achieve same operation. Back Gate of N2 brings N2 in partial conduction mode when logic high presents at output node which results in potential of (Vdd-Vtn) at Vx. The second modification in the Schmitt trigger is introduction of Vb at Back Gate of tail transistor. This modification reduces static leakage current of the cell as FinFET with reverse bias at back gate (Low Power Mode) has much lower Ioff in comparison to shorted gate mode.

5. Schmitt Trigger

Basically Schmitt Trigger circuit is used to convert the analog signal into digital signal. By the Schmitt trigger circuit we can reduce the noise immunity from the circuit and making a circuit in proper shape. Basically the main functioning of Schmitt trigger circuit is to retain its value. There are certain configuration is applied for retaining the value, Just like that the circuit is in non inverting form and the input is higher than a chosen threshold, when this happens the output is high, secondly the input is low at different chosen threshold when this happens the output is low, and lastly the input is between the two levels. This dual threshold phenomenon is known as hysteresis. Because of this process Schmitt trigger creates some memory in the circuit and acts as a Bi-stable Multi vibrator or flip flop. According to the [1] a single cell Schmitt Trigger Based Static RAM using FinFET technology is proposed and analyzed, in comparison of this circuit we have modified the circuit and reduces more leakage current and power consumption because of that the rising price of SRAM is also reduce.

6. Proposed Cell:

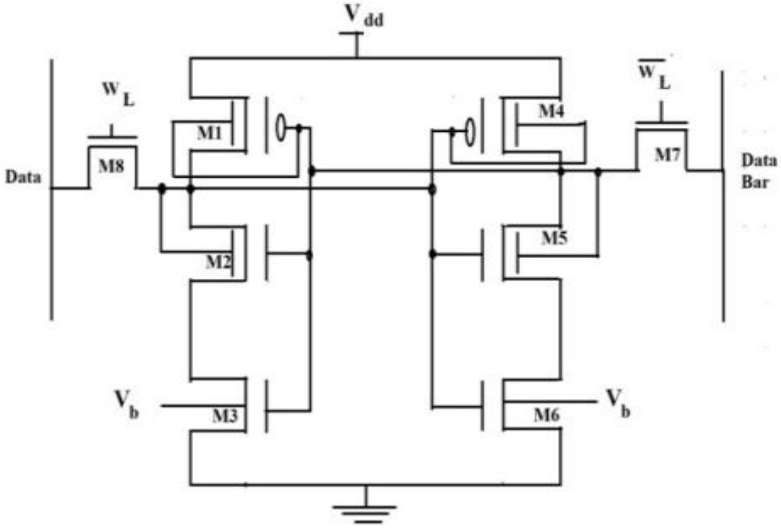

Fig: 3 Proposed SRAM cell

Proposed Schmitt trigger SRAM cell uses modified Schmitt triggers with two access transistors in shorted gate mode as shown in above figure. Proposed cell consists of eight FinFET devices. Devices M1, M4, M7, and M8 are

working in shorted gate mode. M2, M5 are working in independent gate mode and M3, M6 are working in low power mode with a bias of -(Vdd/3). Two Schmitt triggers are formed by devices M4, M5, M6 and M1, M2, M3. These Schmitt triggers make cell more robust to noise which results in low SNM. Schmitt trigger operation is obtained by connecting back gate of M2, M5 to Q and Qb respectively. Connecting back gate to Q and Qb results in partial conduction of device when back gate is at logic high. This partial conduction puts node Vx1/Vx2 at Vdd-Vtn when Q/Qb is high. This makes threshold of half cell consisting of M1, M2, M3 or M4, M5, M6 high which decreases SNM of cell in hold mode. The lower transistors M3 and M6 are provided a bias of -(Vdd/3) at back gate. This reverse bias suppresses the leakage current which results in low power consumption in hold mode. SPICE simulations were carried out to analyze performance parameters of the proposed cell. Value of Vb in simulations was fixed at -(VDD/3) i.e. for VDD=1.8, Vb= -0.6V.

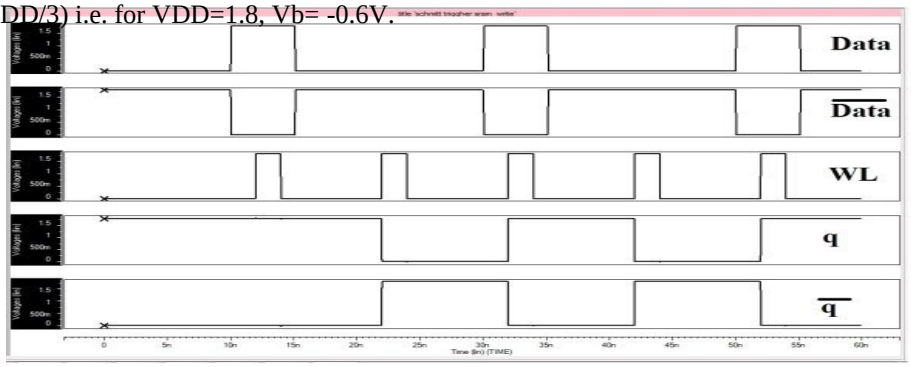

Fig 4: Write Operations

Fig 4 above shows waveforms of write operation on proposed SRAM cell. Logic 1 and Logic 0 are alternatively being written in the presented simulations. Read operation on cell was performed using complete pre-charge and sense amplifier setup. Latch based sense amplifier was use in the setup. Fig 5 below shows read operation on the cell with Pre-charge (Prech), Word line (WL), Sense amplifier enable (SE) signals.

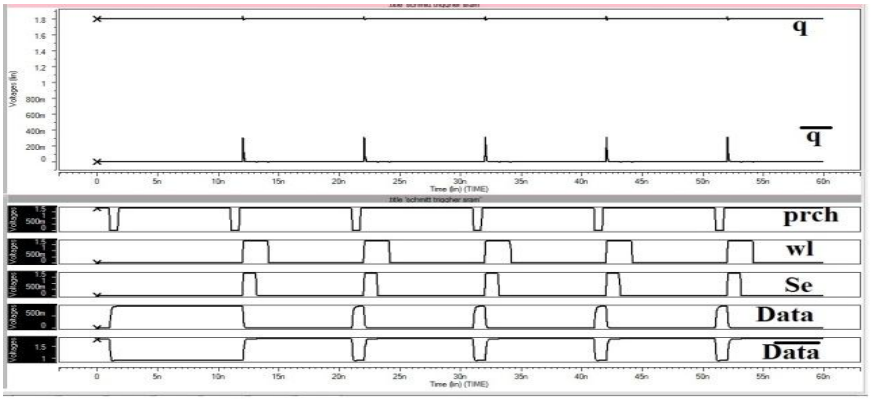

Fig 5: Read Operations

SNM of the proposed cell at different supply voltages is shown in Table.1. The static noise margin is calculated for proposed SRAM, ST SRAM and 6T SRAM and found that the read stability of proposed SRAM is much better than the others.

Table 1: Comparison of Schmitt Trigger SRAM, 6T SRAM and Proposed SRAM

Vdd	SNM 6T SRAM(V)	SNM ST SRAM(V)	SNM Proposed SRAM

1.8	0.175	0.25	0.62
1.6	0.1	0.2	0.56
1.4	0.1	0.2	0.56
1.2	0.06	0.15	0.52
1.0	0.05	0.1	0.42
0.8	0.04	0.08	0.32
0.6	0.03	0.04	0.24
0.4	0.0012	0.025	0.2
0.2	Read Failure	0.012	____

Butterfly curves for SNM at1V, 1.4V and 1.8V are shown in Fig6, Fig 7 and in Fig 8. For calculating the SNM correctly we have to reduce the Vdd step by step.

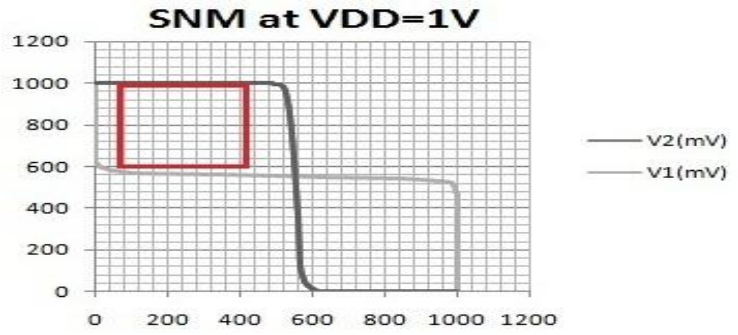

Fig 6: SNM at Vdd 1V

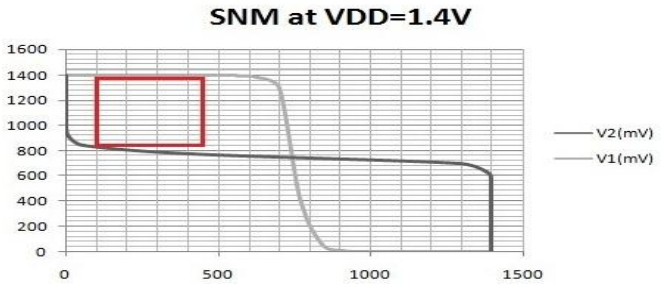

Fig 7: SNM at Vdd 1.4V

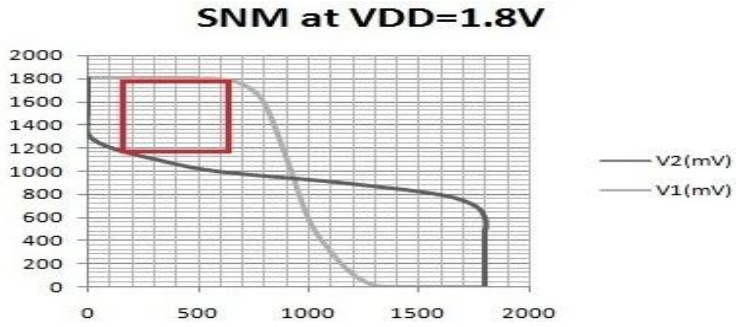

Fig 8: SNM at Vdd 1.

7. Results and Comparisons:

Table 2: Comparison of Power Consumption

Types	Read	Write	Static
6T SRAM	32ps	23ps	____
Schmitt Trigger SRAM[1]	7ps	6ps	____
Proposed SRAM	2.73ps	5.11ps	0.10ps

II shows the comparison between proposed SRAM, Schmitt trigger SRAM and 6T SRAM cell which indicated the considerable reduction in power consumption. Access time for the cells is also measured by simulation which is done by the Synopsis HSPICE tool. The proposed cell shows approx 60% improvement in read delay, and approx 15% in write delay.

8. Conclusion:

The Schmitt Trigger circuit based SRAM is simulated on 32nm FinFET technology which is very well presented in this research paper. The main objective this proposed was to minimize the noise margin which is also followed by the increment in read stability and mitigation of leakage current. The SRAM used in this work is considerably improved when we compare it to the available works, further more the read write stability can be carried in the cell for further enhancement in the cell.

References:

[1] Vasundara Patel K. S., Harsha N. Bhushan, Kiran G. Gadag, Nischal Prasad B. N., Mohmmed Haroon "Schmitt Trigger Based SRAM Using FinFET Technology- Shorted Gate Mode", World Academy of Science, Engineering and Technology International Journal of Computer, Electrical, Automation, Control and Information Engineering Vol:8, No:2, 2014.

[2] Poljak, M., Suligoj, T. ; Jovanovic, V., "Modeling study on carrier mobility in ultra-thin body FinFETs with circuit-level implications", pp: 242-245, ESSDERC, 2010.

[3] Prateek Mishra, AnishMuttreja, and Niraj K. Jha"FinFET Circuit Design", Nano Electronics circuit design, 2011, Springer, pp. 23-54

[4] Vimal Kishore Yadav, Pratiksha Singh Gaur, Sucheta Yadav, "Impending Form Interpretations for Delay to Ramp and Step Input On-Chip VLSI RLC Annex ", "International Journal of Advanced Research in Computer and Communication Engineering(IJARCCE)", vol. 3, Issue 11, ISSN (Online) : 2278-1021,ISSN (Print) : 2319-5940,2014

[5] Young Bok Kim, , Yong-Bin Kim, Fabrizio Lombardi, "New SRAM cell design for low power and high reliability using 32nm independent gate FinFET technology", "IEEE International Workshop on Design and Test of Nano Devices, Circuits and Systems, 2008)", ISBN 978-0-7695-3379-7, 2008

[6] Deeksha Anandani, , Anurag Kumar, V S Kanchana Bhaaskaran, "Gating techniques for 6T SRAM cell using different modes of FinFET", "Advances in Computing, Communications and Informatics (ICACCI), 2015 International Conference on)", ISBN 978-1-4799-8790-0, 2015

[7] Vimal Kishore Yadav, Priyanka Thapak, Sucheta Yadav, "Effect of Ramp Input on RLC Interconnect In Modern VLSI Design", "International Journal of Scientific Research Engineering & Technology (IJSRET)", vol. 3, Issue 8, ISSN 2278 – 0882,2014

[8] Vikas Maheshwari, Shruti Gupta, Kapil Khare, Vimal Yadav, Rajib Kar, Durbadal Mandal, Anup Kr. Bhattacharjee, "Efficient Coupled Noise Estimation for RLC On-Chip Interconnect", IEEE Symposium on Humanities, Science and Engineering Research (SHUSER-2012), Kuala Lumpur, Malaysia, pp. 1125-1129,June 24-27, 2012.

[9] Vikas Maheshwari, Prabhakar Sharma, Alka Goyal, Vimal K Yadav, Sampath Kumar, "Closed Form Expressions for Delay to Ramp Inputs for On-Chip VLSI RC Interconnect", National Conference on Emerging Trends in Electrical, Instrumentation & Communication Engineering, vol. 4, Issue 7 ISSN 2222-1727, (Paper) ISSN 2222-2871 (Online), 2013.