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GATED BODY-BIASED FULL ADDER

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Abstract

As technology advances into the lower nanometer values, power and delay becomes important parameters to increase the efficiency of the circuit. To reduce the sub-threshold leakage power dissipation in standby mode several low power techniques for CMOS circuits namely drain gating, power gating, drain-header and power-footer gating (DHPF), drain-footer and power-header gating (DFPH) are studied and high speed techniques are achieved by modifying drain gating technique and its variant circuits by adding an additional NMOS sleep transistor at the output node which helps in improvement of switching time are studied. The speed of operation of the circuit is improved by applying Gate Level Body Biasing (GLBB) to the design. Implementation of GLBB technique to the existing design proves to be very efficient in terms of speed. Performance parameters such as average power and average propagation delay are compared using existing and proposed techniques for a full adder circuit. The full adder circuit with various low power techniques are tools in 180nm technology. The circuit is simulated using Cadence Spectre tool. The circuit operates with more speediness after applying biasing and found increase in speed by 15%.

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Keywords: Delay; Power Gating; Body Biasing

1. Introduction

In today's world, integration of more number of transistors on a single chip is achieved by VLSI designing. With advancement in technology, it has been observed that electronic circuits have become more Compaq due to the reduction in size of transistors that indeed lowers the supply voltages, thus decreasing the power dissipation. By varying the threshold voltage with respect to supply voltage it has been found that transistor switching speed could be maintained. As a result the leakage current increases with the upgrade in technology which in turn power

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dissipation increases proportionally. In order to reduce total leakage, new low power techniques need to be developed. The leakage current is of two types, the first one is sub-threshold current, which is due to the carrier diffusion between source and drain of the off transistors coming to next reverse-bias diode current, which is due to the stored charge between the drain and bulk of active transistors. With the aim to decrease the leakage current in CMOS circuits, many techniques have evolved among which Power gating[1] and stacking effect[2] are the most prominent ones. Stacking technique reduces the leakage current but increases the delay of the logic circuit. Whereas when it comes to Power gating technique it involves usage of two sleep transistors among which one is connected between the power supply and pull-up network (PUN) and the other between the pull-down network(PDN) and ground. They are turned on the circuit is in active mode and they are off in standby mode to conserve the leakage power in the circuit. Apart from these two techniques another technique has been developed called the Multi-threshold-CMOS (MTCMOS) technique [3] which was found to be successful in reducing the leakage current to a further extent. In MTCMOS technique, high V_{th} sleep transistors are added in the circuit whereas PUN and PDN use low V_{th} devices. In dual threshold circuits [4], low V_{th} devices are used to reduce delay and high V_{th} devices are used to reduce the leakage current in the circuitry. Another effective technique to achieve decreasing of leakage power consumption is drain gating and its variant circuits [5].

2. Literature Survey

There are many techniques to implement any circuit with low-power and high speed. Drain gating technique [5] can be implemented by using two sleep transistors which are placed between PUN and PDN. Among which PMOS transistor with sleep input (S) is connected between PUN and output node, whereas NMOS transistor with sleep input (S') is inserted between the output node and PDN. The working is explained as follows. When the circuit is in active mode both the sleep transistors are turned on resulting in low resistance conducting path while in the case of standby mode both the transistors are switched off to reduce the standby power. With the help of drain gating technique many techniques has proposed and implemented by re-arranging of sleep transistors. The other techniques are drain-header and power-footer gating (DHPF), power gating and drain-footer and power-header gating (DFPH). In DHPF, a NMOS sleep transistor with input (S') is inserted between the PDN and ground rail and a PMOS sleep transistor with input (S) is inserted between PUN and PDN i.e., at output node. Power gating consists of a NMOS sleep transistor with input (S') between the PDN and ground rail, whereas PMOS sleep transistor with input (S) between the power supply and the PUN. Whereas in the DFPH, an NMOS sleep transistor with input (S') is added between output node and PDN and a PMOS sleep transistor with input (S) is added between the power supply and PUN. All these techniques are aimed at reducing the leakage and delay. Further advanced research showed that the speed of the logic circuit could be further enhanced by adding an extra circuitry i.e., an additional sleep transistor with sleep input (S) when connected at the output node parallel to NMOS sleep transistor and PDN would reduce the propagation delay. This can be explained as follows during the active mode, when the logic circuit evaluates the circuit output, the added NMOS sleep transistor(S) provides an additional discharging path in the circuit. This added transistor helps in speedy evaluation, hence providing higher speed.

3. Proposed System

3.1. HYBRID FULL ADDER

As stated, earlier techniques consume more power, in order to decrease power use weak NMOS transistors. This is achieved by decreasing the channel width of the transistor. The default width of transistor is 2um in 180nm technology. It is observed decrease in power by keeping channel width of NMOS transistor as 1um without altering the width of PMOS transistors. The results are compared with previous techniques and tabulated in TABLE 1.

TABLE 1: Average Power (uW) of full adder and hybrid full adder

Technique	Without changing width	With changing width
DG	36.13	25.11
PG	28.78	20.17
DHPF	35.57	23.17

DFPH	32.88	22.36
HS-DG	38.04	26.22
HS-PG	30.80	21.47
HS-DHPF	34.25	24.10
HS-DFPH	34.89	23.45

3.2 GLBB FULL ADDER

The improvement in speed of full adder in circuit has been observed using body-body biasing scheme [7]. In this technique biasing circuit consists of two blocks. One is logical circuit which is used for logical functionality and the other is body biasing generator (BBG). The output of logical block is given as input to the BBG which in turn generates body voltage (VB) and applied to the devices used in the circuit design. This biasing voltage is considered as important parameter in minimization of delay. The BBG section consists of two transistors PMOS and NMOS. Drains of these two transistors are connected to GND (logic 0) and high voltage (logic 1) and substrates are connected to high voltage (logic 1) and GND (logic 0) respectively. Body voltage (VB) is generated at common source of these two transistors. When the output of logical circuit (VOUT) i.e.; input of BBG is high then BBG block transfers high voltage on VB which in turn switching of pull-down network increases. Similarly when VOUT is low then VB is low which makes pull-up network switching time faster. As a result there is an improvement in the total speed of the circuit design due to forward body biasing mechanism. Due to body induced RC delay, the transition of the input signals is not slowed down. Because of VB voltage before inputs' transition, high capacitive load of BBG does not constitute a speed bottleneck. We design circuit by using two BBG. The inputs of these two BBG are COUT (carry) and S (sum) which generates two biasing voltages namely VB1 and VB2 respectively. In this, we connected substrates of carry generated block along with sleep transistors to VB1 and substrates of sum generated block including sleep transistors is connected to VB2.

3.3 GATED BODY-BIASED FULL ADDER

The proposed full adder is implemented by applying body-biasing scheme for eight different techniques namely drain gating (DG), power gating (PG), drain-header and power-footer gating (DHPF), drain-footer and power-header

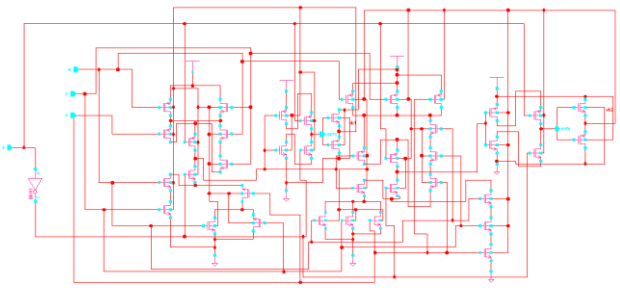


Fig 1: Body-biased drain gating

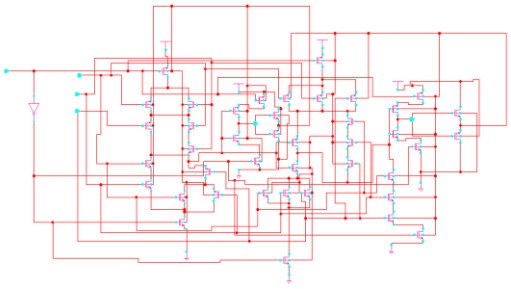


Fig 2: Body-biased power gating

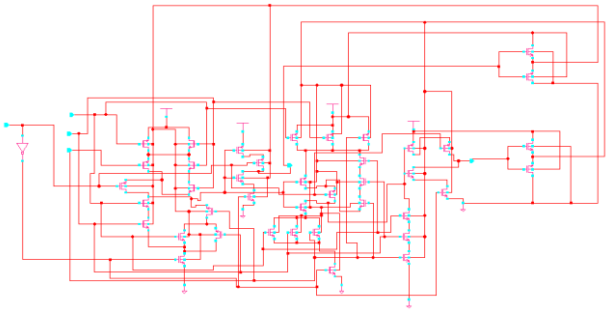


Fig 3: Body-biased DHPF

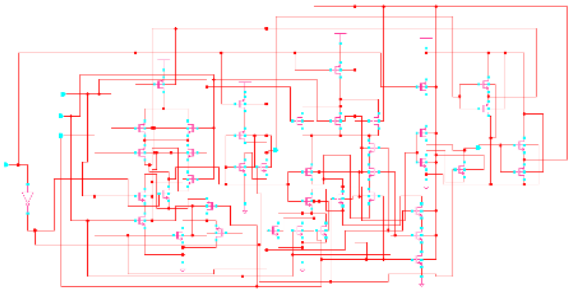


Fig 4: Body-biased DFPH

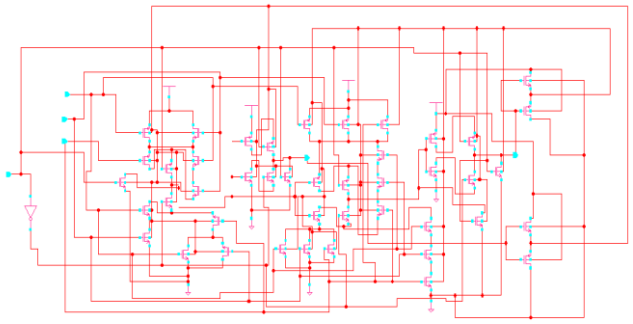


Fig 5: Body-biased HS-drain gating

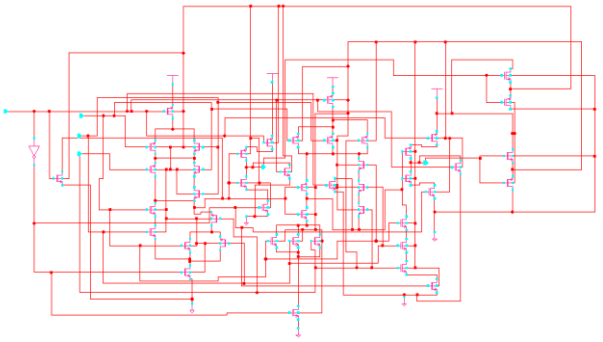


Fig 6: Body-biased HS-power gating

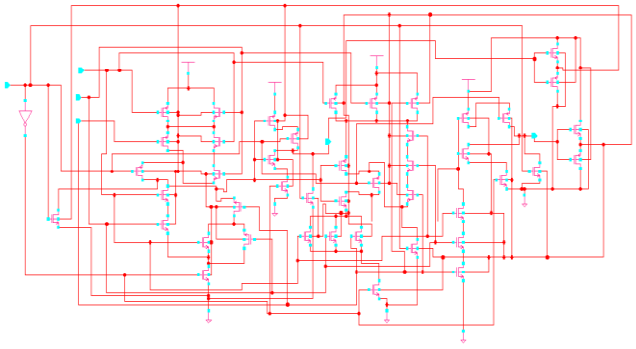


Fig 7: Body-biased HS-DHPF

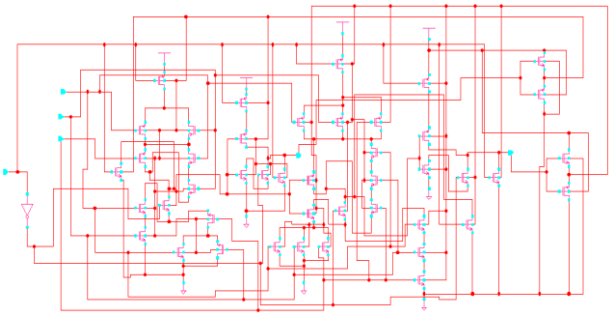


Fig 8: Body-biased HS-DFPH

gating (DFPH), high-speed drain gating (HS-DG), high-speed power gating (HS-PG), high-speed drain-header and power-footer gating (HS-DHPF), high-speed drain-footer and power-header gating (HS-DFPH) as shown in Fig 1 - 8 respectively. The improvement in speed is observed by using this technique. Comparison between body- biasing technique and gating techniques [6] is done and the results are tabulated in TABLE 2 (without body-biasing), TABLE 3 (with body-biasing) respectively

TABLE 2: Delay and Average Power of adder without Body-Biasing

Parameter	a*-Cout (pS)	a*-Sum (pS)	Power (uW)
DG	155.4	155.5	36.13
PG	98.84	117.2	28.78
DHPF	119.9	119.2	35.57
DFPH	131.4	141.4	32.88
HS-DG	172.3	174.7	38.04
HS-PG	116.6	138.6	30.80
HS-DHPF	137.2	119.2	34.25
HS-DFPH	148.3	162.3	34.89

TABLE 3: Delay and Average Power of adder with Body-Biasing

Parameter	a*-Cout (pS)	a*-Sum (pS)	Power (uW)
DG	134.5	144.7	212.8
PG	91.75	116.8	121.5
DHPF	107.3	77.71	211.0
DFPH	123.1	133.5	198.4
HS-DG	146.8	160.3	291.7
HS-PG	104.5	133.4	199.1
HS-DHPF	116.4	116.4	212.7
HS-DFPH	138.2	152.7	269.2

3.4 BODY-BIASED HYBRID FULL ADDER

As BBG block in GLBB technique requires additional two transistors so that four transistors are added more in our proposed system. As a result transistor count increases and thus power consumption increases. In order to decrease power we introducing one more technique namely self-biased hybrid full adder. In this technique change in width of transistor takes place i.e., applying hybrid technique (NMOS transistor width 1um) to body-biased full adder. By implementing this we observed decrease in power compared with GLBB technique. The comparison between self-biased and self-biased hybrid technique is done and depicted in TABLE 4.

TABLE 4: Average Power (uW) of body-biased adders

Technique	Body-biased full adder	Body-biased hybrid full adder
DG	291.7	185.0
PG	199.1	126.7
DHPF	212.7	133.6
DFPH	269.2	173.4
HS-DG	212.8	133.9
HS-PG	121.5	85.27
HS-DHPF	211.0	79.76
HS-DFPH	198.4	126.3

RESULTS AND DISCUSSIONS

The proposed techniques are implemented by using technology gdpk180. The simulation was performed using Cadence spectra tool with supply voltage 1.8v in 180nm technology. The proposed full adder circuit is compared with previous full adder design styles which are implemented by using different gating techniques [6]. The circuits of other full adders were designed and verified in cadence spectra tool in 180nm technology. So, the paper can be authentically compared the proposed full adder designs with other full adder circuits reported in [6]. The Body biased full adder circuit with various gating techniques is simulated using cadence spectra tool and the functionality of the proposed system is verified. Simulation results of Body biased DG hybrid full adder in Fig9, Body biased PG hybrid full adder in Fig 10, Body biased DHPF hybrid full adder in Fig 11, Body biased DFPH hybrid full adder in Fig 12, Body biased HS-DG hybrid full adder in Fig 13, Body biased HS-PG hybrid full adder in Fig 14, Body biased HS-DHPF hybrid full adder in Fig 15, and Body biased HS-DFPH hybrid full adder in Fig 16 are shown.

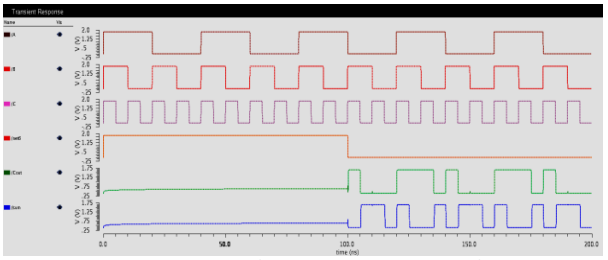


Fig 9: Simulation results of body-biased DG hybrid full adder

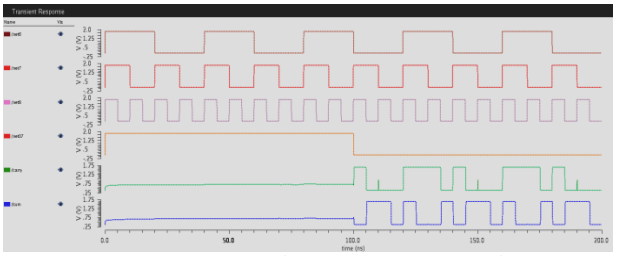


Fig 10: Simulation results of body-biased PG hybrid full adder

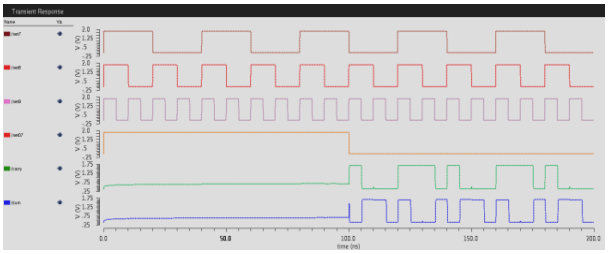


Fig 11: Simulation results of body-biased DHPF hybrid full adder

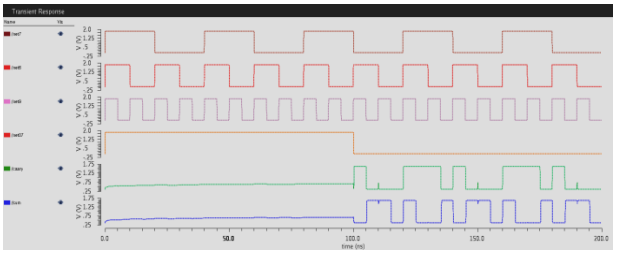
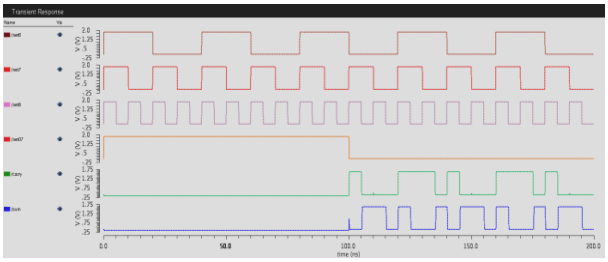


Fig 12: Simulation results of body-biased DFPH hybrid full adder



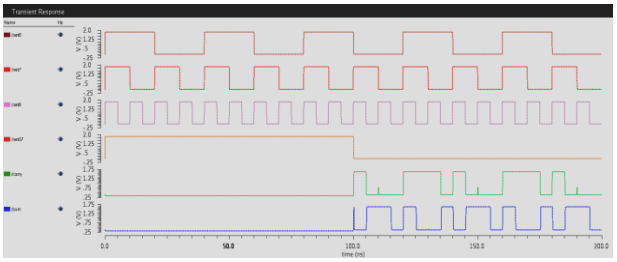


Fig 13: Simulation results of body-biased HS-DG hybrid full adder

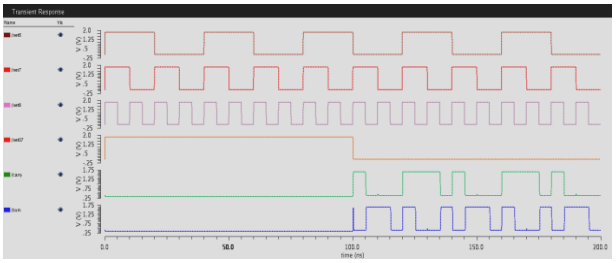


Fig 14: Simulation results of body-biased HS-PG hybrid full adder

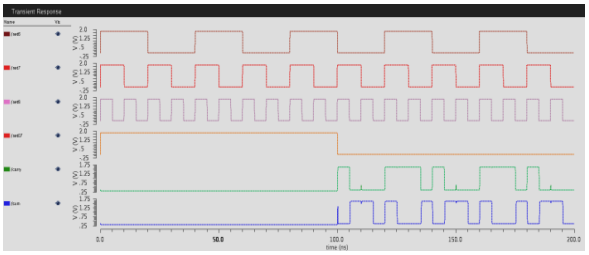


Fig 15: Simulation results of body-biased HS-DHPF hybrid full adder

Fig 16: Simulation results of body-biased HS-DFPH hybrid full adder

4. Conclusion

In this paper, hybrid full adder, body-biased full adder and body-biased hybrid full adder circuit has been proposed. The simulation results were carried out using cadence spectra tool with 180nm technology and compared with the other full adder circuits which are implemented by gating techniques. The simulation results show that the proposed adder offers improved average delay and average power with the earlier reports. The circuit operates with more speediness after applying biasing and found increase in speed by 15%.

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