Available online at www.sciencedirect.com

ScienceDirect

Materials Today: Proceedings XX (2016) XXX–XXX

materialstoday: PROCEEDINGS

www.materialstoday.com/proceedings

PMME 2016

Investigations on the Nitride Interface Engineering at HfO_2/Ge stacks for MOS devices

G. Venkata Rao[a], M.Kumar[a], T.V.Rajesh[a], D.V. Rama Koti Reddy[b], D.Anjaneyulu[c], B. Sainath[d] and S.V.Jagadeesh Chandra[a]*

[a]*Department of Electronics and Communication Engineering, Lakireddy Bali Reddy College of Engineering, Mylavaram-521 230, Andhra Pradesh, India*

[b]*Department of Instrument Technology, Andhra University. Visakhapatnam-530003, Andhra Pradesh, India.*

[c]*Department of Electronics and Communication Engineering, CMR Institute of Technology, Kandlakoya, Medchal, Hyderabad-501401, Telangana, India.*

[d]*Department of Electrnonics and Communication Engineering, Madanapalli Institute of Technology and Science, Madanapalli, Andhra Pradesh, India.*

Abstract

Passivation layer influenced structural and electrical properties of Ge MOS devices have been reported. Nitride layer was deposited on Ge substrate with rapid thermal annealing before HfO_2 deposition. XRD spectra revealed that there was no difractional peak related to HfO_2 on Ge substrate after annealing. HREM images showed that there was clear interface at annealed HfO_2/Ge stacks. C-V plots revealed that, intentionally formed interfacial nitride layer showed significant improvement in the interface quality between HfO_2 and Ge. I-V characteristics showed that Ge devices showed about one order lower leakage current densities than Si devices. All of these observations might be due to the process of surface passivation on Ge substrate.

Selection and Peer-review under responsibility of International Conference on Processing of Materials, Minerals and Energy (July 29th – 30th) 2016, Ongole, Andhra Pradesh, India.

Keywords: Germanium, Rapid thermal process, Nitride layer, Hafnium oxide, Metal-oxide- Semiconductor device

1.Introduction : The demand for low power consumption, alternative channel material for high performance CMOS devices and introduction of high-k gate dielectrics in Si technology has gained significant interest towards Ge [1, 2]. The smaller band gap of Ge (~0.66 eV) potentially allows for lower contact resistances as compared to Si (~1.1 eV) due to barrier height reduction and hence more suitable for voltage (V_{DD}) scaling [3]. To realize the applications of

* Corresponding author. Tel.: +08659-222933 (Ext:416); fax: +08659-222931.
E-mail address: svjchandra@lbrce.ac.in

Selection and Peer-review under responsibility of International Conference on Processing of Materials, Minerals and Energy (July 29th – 30th) 2016, Ongole, Andhra Pradesh, India.

high performance Ge MOS devices, the key issue is the quality of interface between the high-k dielectrics and Ge [4]. Deposition of a high-k gate dielectric on Ge exhibits high interfacial trap density, poor electrical characteristics and high gate leakage current densities [5, 6]. The undesirable surface properties and water soluble native oxides of Ge leading to poor interface quality between oxide and Ge [7]. Different interface passivation techniques such as nitridation (Ge_xN_y, AlN, TaON and GeO_xN_y), sulfur passivation or silicon nitridation (SiN) have been employed to obtain stable interface at oxide/Ge stacks [8-10]. Among these passivation layers, germanium nitride (Ge_xN_y) might be more stable in terms of thermal and chemical properties [11]. The stable passivation layer between oxide and Ge exhibits low interfacial trap density, good electrical characteristics and low gate leakage currents [12]. The selection of high-k gate dielectric material involves several aspects with respect to the channel material [9]. The most investigated high-k materials for gate dielectrics are TiO_2, Ta_2O_5, HfO_2, ZrO_2, Si_3N_4, Al_2O_3 and CeO_2. Among various high-k dielectrics, HfO_2 is the most promising gate dielectric because of its relative high-k value, wide band gap, high thermal stability, breakdown electric field (E_{BD}), large conduction band and valence band offsets [13]. Besides, HfO_2 has high free energy of reaction with substrate to meet the scaling requirements as mentioned in the International Technology Roadmap [14]. On the other hand, high vacuum work function metals have to be chosen for metal gate electrode for MOS devices. The chrome-gold (Cr- Au) is used as the top gate electrode. In this work, we have performed the thermal nitridation of Ge in NH_3 ambient using rapid thermal processing (RTP) for the passivation of germanium surface. The crystallographic structure, microstructure and electrical properties on the basis of interface between HfO_2/Ge stack were investigated and compared with well established HfO_2/Si stack.

2. Experimental details

The p-type Ge <100> substrates with resistivity of 0.01 - 0.1 Ω-cm was used for the fabrication of MOS devices. Ge substrate was cleaned by cyclic HF:DI dips to remove impurities and native oxides. After hydrochloric acid treatment for surface passivation, the Ge samples were immediately loaded into a rapid thermal processing (RTP) chamber for growth of the passivation layer. Germanium nitride (Ge_3N_4) passivation layer was grown by RTP using ammonia (NH_3) at a temperature of 573 $^{\circ}$C. The growth of Ge_3N_4 layer was confirmed by the X-ray photoelectron spectroscopy (XPS) studies (not shown here). The physical thickness of Ge_3N_4 layer determined using ellipsometry was about 0.9 nm. After surface passivation, Ge was loaded into atomic layer deposition (ALD) chamber to deposit HfO_2 film. HfO_2 layer was deposited using tetrakis (Diethylamide) Hafnium (Hf $(NMe_2)_4$) as the precursor and H_2O sources at a wafer temperature of 200°C with a thickness of 6 nm. HfO_2/Ge stacks were annealed at 300^0 C and 400°C in forming gas followed by oxygen environment. The crystallographic structure o f the HfO_2 films was characterized by Rigaku Smart Lab 3 KW X-ray diffractometer (XRD). The microstructure of HfO_2/Ge was examined using PHILIPS CM 200 high resolution electron microscopy (HREM). For a gate electrode, a 100 nm thick Au films were deposited on a 30 nm thick Chromium layer for better adhesion using electron beam evaporation. After gate patterning with dimensions 300 µm × 300 µm using liftoff lithography, and resulting devices referred to in this paper as Ge devices. For comparison, Au/Cr/HfO_2 gate stacks were formed on chemically cleaned p-type Si <100> wafers using the same fabrication conditions and the resulting devices are referred in this paper as the Si devices. After removing the native oxide at the back side of Ge and Si substrates a 50 nm thick Al films were deposited as back contact. The capacitance - voltage (C-V) characteristics were measured at100 KHz using a Keithley 4200-SCS precision LCR meter. Current – voltage (I-V) characteristics were determined using a precision semiconductor parameter analyzer (Agilent 4156C).

3. Results and Discussion

Figure 1 shows the XRD patterns of HfO_2 on Ge and Si MOS devices. There are no diffraction peaks for as-deposited HfO_2 film on both Ge and Si indicated that the as-grown layers were amorphous in nature. After annealing at 300^{o}C, there was a peak at around 32^{o} in both Ge and Si devices. In the case of Si devices, the peak observed at around 32 ^{o} might be associated with the tetragonal phase of HfO_2 layer with an <hkl> value of <111> [15]. The peak intensity was increased by increasing the annealing temperature to 400^{o}C. On the other hand, the peak observed in Ge after annealing at around 32^{o} could be related to Ge <200> peak [17]. It seems that there was no difractional peak related to HfO_2 on Ge substrate. It could be due to the intentionally grown interface nitride layer on Ge i.e. Ge_3N_4. The presence of Ge_3N_4 was also confirmed by the XPS studies (which were not shown here). In particular, Ge_3N_4 layer increases the crystallization temperature of high-k dielectrics and acts as a crystallization inhibitor. Besides, the intentionally grown nitride layer can also suppress the growth of microstructure and unstable

GeO_x layer on Ge [17].

Figure 2 shows the cross-sectional high-resolution electron microscope images of Ge and Si devices before annealing. It is clear from figure 2(a) that, there was a clear interface between Ge and HfO_2 with thickness of around 0.9 nm. The thickness of the passivated interfacial Ge_3N_4 layer also measured using ellipsometry. It might be a significant approach to have such a thin stable layer at Ge/high-k stacks. The thickness of the measured oxide layer before annealing was 6 nm (fig. 2a), and the same was increased to about 0.4 nm in Ge devices after annealing (not shown here). It might be due to the strengthening of interfacial nitride layer at the bottom stack. It could also be the reason to be HfO_2 in the amorphous on Ge after annealing, since nitride layer is a significant inhibitor for crystallization effect [17].

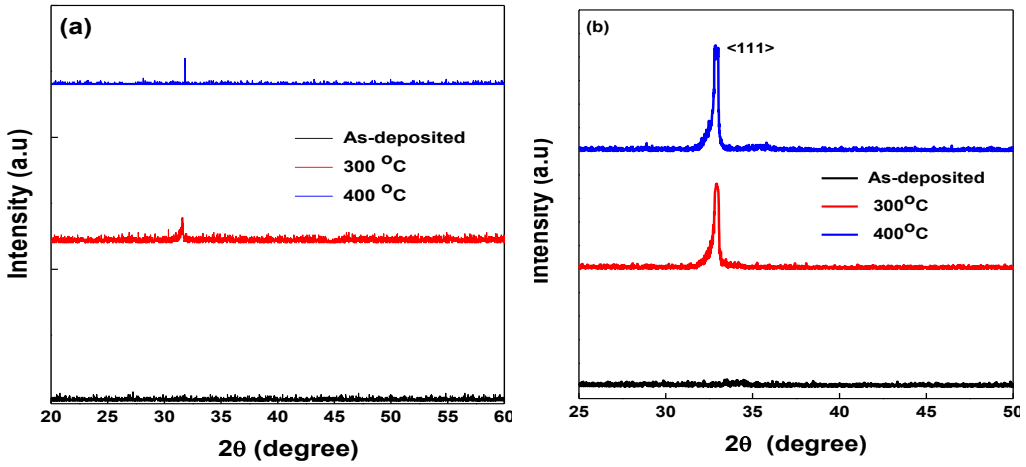

Figure 1: X-Ray Diffraction Spectra of (a) Ge (b) Si devices

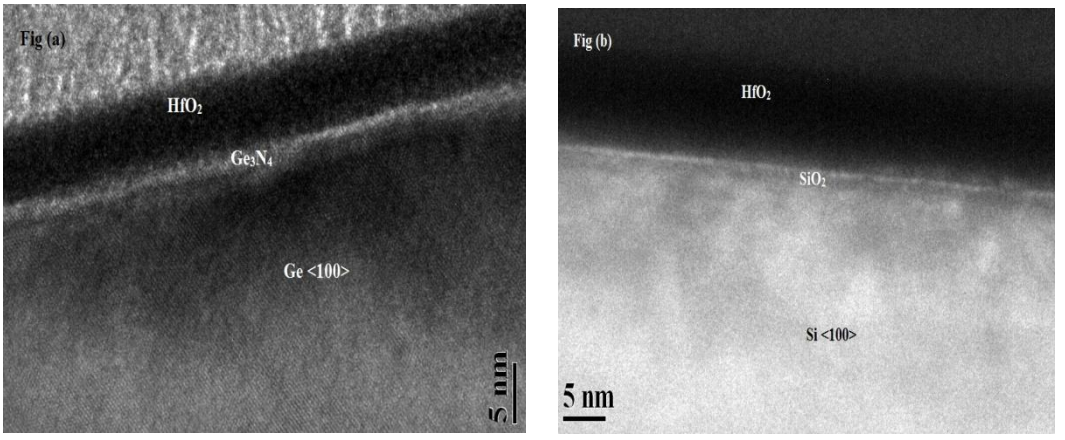

Figure 2: HREM images taken from (a) Ge devices and (b) Si devices before annealing

Capacitance -Voltage characteristics of as-deposited Ge and Si devices are shown in Figure 3. Figure 3a explained that the accumulation capacitance value is significantly higher in as-deposited Si devices than Ge devices; it could be due to the intentional growth of nitride layer on Ge surface. Besides, the depletion and deep depletion regions of both devices showed small bumps/kinks in the path of the curves [13]. Whereas, Ge devices showed more intensive bump in depletion regions, relatively when compare with the Si devices. These observations might be due to the low quality of interface at HfO_2/Ge stacks [18]. It is quite interesting here from our previous studies that the intensity of

stretch and kinks/bumps in the depletion region is significantly reduced in the present study in as-deposited Ge devices too [19]. The reason for this observation is the introduction of interfacial nitride layer resulting to improvement in the interface quality. It is clear from Ge devices (Figure 3b) that the accumulation capacitance is reduced significantly after annealing at 300°C, while the same does not has significant influence after increasing the annealing temperature to 400°C. The sudden decrease in the accumulation capacitance after annealing at 300°C, might be due to the strengthening of the passivated low-k germanium nitride (Ge_3N_4) layer. On the other hand, there was an improvement in the interface quality by showing the reduction in the stretch at depletion region in annealed devices (Figure 3b), eventually; the kinks/bumps in the depletion region were completely disappeared with more reduced depletion region after increase in the annealing temperature to 400°C [17,20]. The reason for this observation could be the reduction in the interface state density level at HfO_2/Ge stacks. Whereas, in the case of Si devices (Figure 3c), there was no much difference in accumulation capacitance value and improvement in the interface quality after annealing at 300 and 400°C, since there were not only small bumps/kinks in the deep depletion but also no significant improvement in the path of depletion region [14].

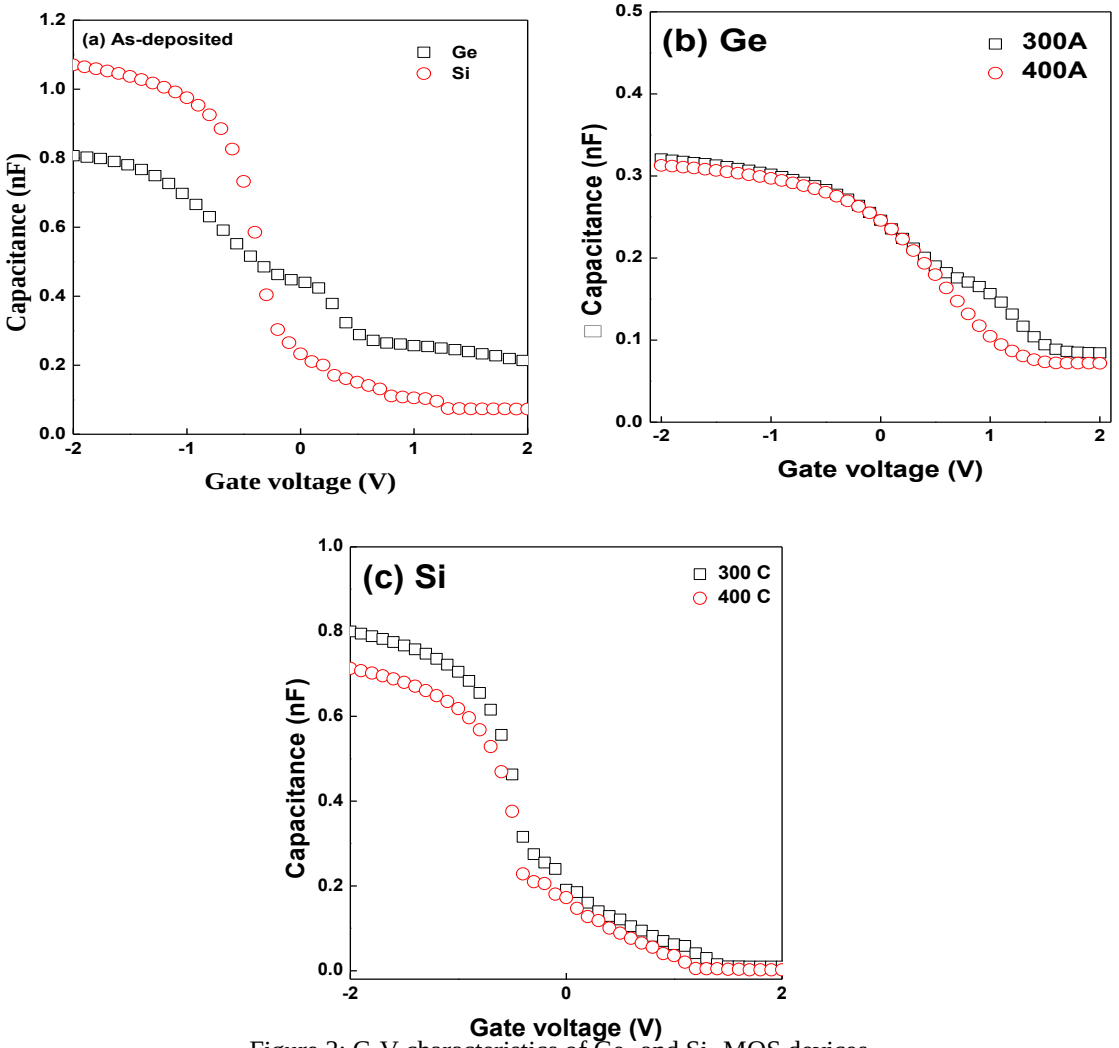

Figure 3: C-V characteristics of Ge- and Si- MOS devices

Figure 4 illustrates more evidently about the interface quality at annealed Ge- and Si- devices by extracting C-V curves at 10 and 100 KHz frequencies. Annealing temperature of 300°C was not sufficient to improve the interface quality in Ge and Si devices (Figure 4a), but the temperature 400 °C showed significant improvement in Ge devices

(Figure 4b). But, there was no much improvement in the nature of C-V plots in the annealed Si-devices. In addition, there was noticeable frequency dispersion in the Ge devices relatively compared with Si devices [14]; it might be owing to the strengthening of intentional nitride layer. It means that during the annealing process interfacial nitride layer plays major role as inhibitor for transition to crystallization and to improve the interface quality in Ge devices [18]. On the other hand, it was direct evidence from the C-V plots that there was perceptible role of series resistance in Ge devices. It means that there was distinguished interface with strengthened low-k interfacial layer at HfO_2/Ge stack, leading to low accumulation capacitance values in annealed devices as we reported earlier. Additionally, to verify in particular the interface quality of HfO_2 films, we observed the behavior of hysteresis curves (not shown here) in both Ge and Si MOS devices by performing bidirectional scans (accumulation to inversion and vice versa). Ge devices showed much lower hysteresis loop than Si devices illustrating the effectiveness of the Ge_3N_4 passivation layer between HfO_2 and Ge.

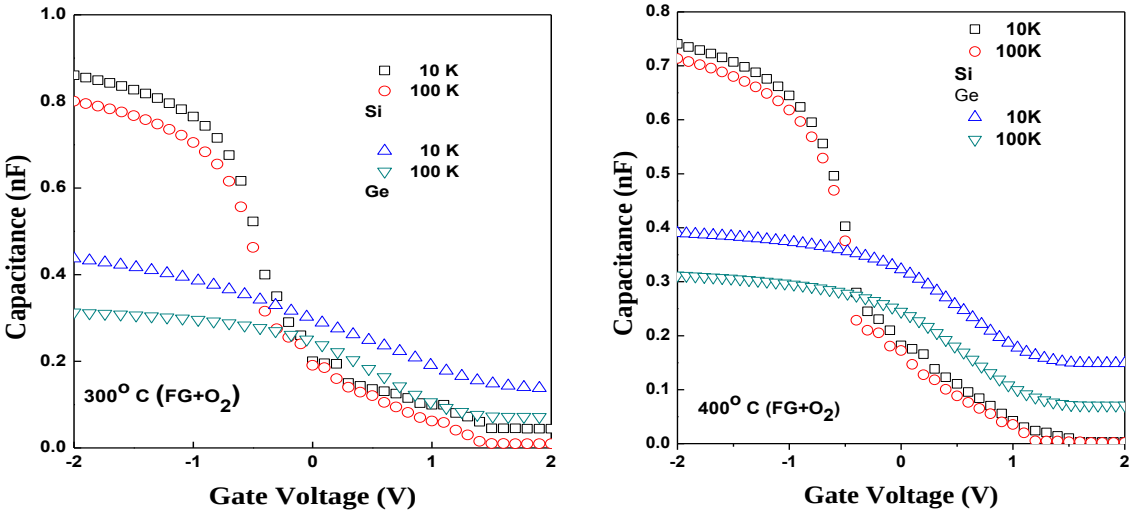

Figure 4: C-V characteristics of annealed at Ge- and Si- MOS devices

Current-Voltage characteristics of Ge and Si MOS devices are shown in Figure 5. In both the devices, there was a decrease in the leakage current density after annealing [14]. The leakage current density in as-deposited Si devices (Figure 5b) at around 0.2 V of applied voltage was ~$5x10^{-3}$ A/cm^2, whereas, in the case of Ge devices (Figure 5a), the same was reduced to two orders, i.e., ~$1x10^{-6}$ A/cm^2. The leakage current density after annealing at 300^{o}C was ~$2.1x10^{-4}$ A/cm^2 in Si- and ~$6.1x10^{-8}$ A/cm^2 in Ge devices. Similarly, the noticed leakage current densities of the Si- and Ge- devices after annealing at 400^{o}C, were ~$1.39x10^{-5}$A/cm^2 and ~$8.2x10^{-9}$ A/cm^2, respectively. This drastic reduction and extremely low value of leakage current density also confirm the growth of good quality of oxide and the oxide charges reduction and are consistent with the results shown [21]. This significance decrease in the current density value could be due to the good quality interfacial layer at HfO_2/Ge stacks.

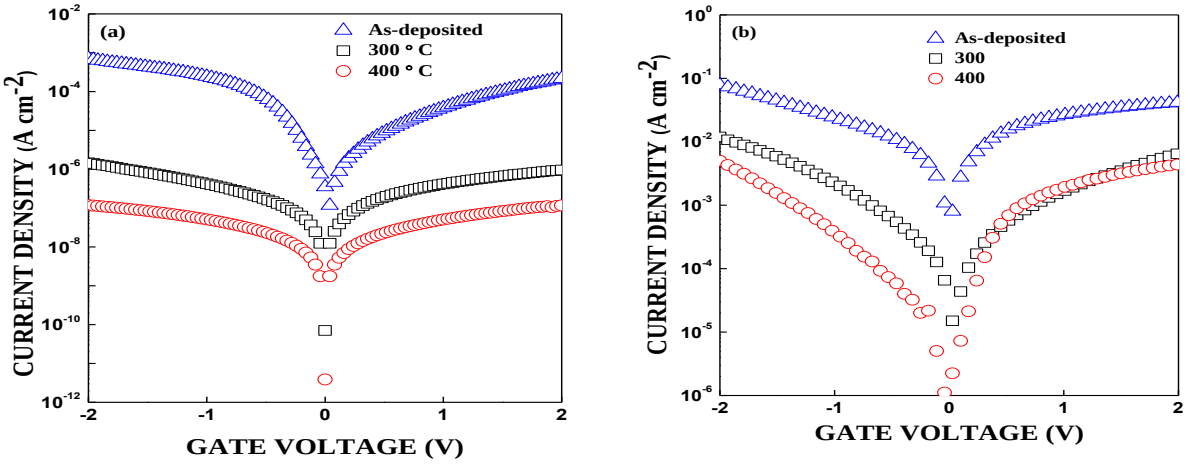

Figure 5: Current-Voltage characteristics of (a) Ge and (b) Si devices

Conclusions

We fabricated HfO_2/Ge MOS devices by depositing intentional nitride (Ge_3N_4) layer on Ge and demonstrated the effect of the annealing ambience on the interface engineering at HfO_2/Ge device, and showed a comparison with Si MOS device. The Ge_3N_4 interlayer can effectively block the transformation of HfO_2 layer from amorphous to crystalline and suppress the growth of unstable GeO_x. The reduction in the accumulation capacitance of annealed Ge MOS device was more when compared to annealed Si MOS device due to the strengthening of low-k interfacial layer beneath the HfO_2. The reliable improvement in the interface quality and electrical properties are neither the presence of bumps/kinks in depletion and inversion regions nor high leakage currents in Ge devices. Hence the post deposition annealing plays a prominent role herein in the reduction of interface states and eventually in the improvement of the interface quality of the MOS devices, resulting to very low leakage currents in Ge devices.

Acknowledgement

This work was carried out with the financial support extended under Indian Nanoelectronics User Program (INUP), Indian Institute of Technology Bombay (IITB), India.

References

1. Shinichi Takagi, Rui Zhang, Junkyo Suh, Sang-Hyeon Kim, Masafumi Yokoyama, Koichi Nishi, Mitsuru Takenaka, III–V/Ge channel MOS device technologies in nano CMOS era, Jap. J. Appl. Phy., **54** (2015) 06FA01-06FA018.
2. H. Shang, M.M. Frank, E.P. Gusev, J.O. Chu, S.W. Bedell, K.W. Guarini, M. Ieong, Germanium channel MOSFETs: Opportunities and challenges. IBM J. Res. Dev. **50** (2006) 377–386.
3. S. Takagi, T. Irisawa, T. Tezuka, T. Numata, S. Nakaharai, N. Hirashita, Y. Moriyama, K. Usuda, E. Toyoda, S. Dissanayake, M. Shichijo, R. Nakane, S. Sugahara, M. Takenaka, N. Sugiyama, Carrier-transport-enhanced channel CMOS for improved power consumption and performance, IEEE Trans. Electron Dev., **55(2)** (2008) 21-39.
4. L.K. Chu, R.L. Chu, T.D. Lin, W.C. Lee, C.A. Lin, M.L. Huang, Y.J. Lee, J. Kwo, M. Hong, Metal-oxide-semiconductor devices with molecular beam epitaxy-grown Y_2O_3 on Ge, J. Crys. Growth, **311(7)** (2009) 2195-2198.
5. E.P. Gusev, Huiling Shang, Matt Copel, M.A. Gribelyuk, C. D'Emic, P. Kozlowski, T. Zabel, Microstructure and thermal stability of HfO_2 gate dielectric deposited on Ge (100), Appl. Phys. Lett., **85(12)** (2004) 2334-2336.
6. C.O. Choi, Shriram Ramanathan, Baylor B. Triplet, Paul C McIntyre, Krishna C. Saraswat, Germanium MOS capacitors incorporating ultrathin high-k gate dielectric, IEEE Electron. Dev. Lett., **23(8)** (2002) 473-475.

7. Jennifer S Hovis, Robert J Hamers, C Michael Greenlief, Preparation of clean and atomically flat germanium (001) surfaces, Surf. Sci., **440(1)** (1999) L815-L819.
8. Zhao Mei, Liang Renrong, Wang Jing, Xu Jun, Effective interface passivation of a Ge/HfO_2 gate stack using ozone pre-gate treatment and ozone ambient annealing, J. Semicon., **34(6)** (2013) 066005 (1-4).
9. Qi Xie, Shaoren Deng, Marc Schaekers, Dennis Lin, Matty Caymax, Annelies Delabie, Xin-Ping Qu, Yu-Long Jiang, Davy Deduytsche, Christophe Detavernier, Germanium surface passivation and atomic layer deposition of high-k dielectrics - a tutorial review on Ge-based MOS capacitors, Semicond. Sci. Tech., **27(7)** (2012) 074012.
10. G. Okamoto, K. Kutsuki, T. Hosoi, T. Shimura, and H. Watanabe, Electrical characteristics of Ge-based metal-insulator-semiconductor devices with Ge_3N_4 dielectrics formed by plasma nitridation, J. Nanosci. Nanotech., **11(4)** (2011) 2856–2860.
11. S. J. Wang, J. W. Chai, J. S. Pan, A. C. H. Huan, Thermal stability and band alignments for Ge3N4 dielectrics on Ge, Appl. Phys. Lett., **89(2)** (2006) 022105 (1-3).
12. Y. Oshima, Y. Sun, D. Kuzum, T. Sugawara, K.C. Saraswat, P. Pianetta, and P.C. Mc Intyre, Chemical bonding, interfaces and defects in hafnium oxide/germanium oxynitride gate stacks on Ge (100), J. Electrochem. Soc., **155** (2008) G304-G309.
13. S.V. Jagadeesh Chandra, M. Jeong, Y.C. Park, J.W. Yoon, C.J. Choi, Effect of Annealing Ambient on Structural and Electrical Properties of Ge-Metal-Oxide-Semiconductor Capacitors with Pt Gate Electrode and HfO_2 Gate Dielectric, Mater. Trans., **52(1)** (2011) 118-123.
14. International Technology Roadmap for Semiconductors, Semiconductor Industry Association, 2009, Available from: <http://www.itrs.net/>.
15. G. He, M. Liu, L.Q. Zhu, M. Chang, Q. Fang and L.D. Zhang, Effect of post-deposition annealing on the thermal stability and structural characteristics of sputtered HfO_2 films on Si (100), Surf. Sci., **576** (2005) 67-75.
16. S.V. Jagadeesh Chandra, P. Sreedhara Reddy, G. Mohan Rao, S. Uthanna, Effect of Postdeposition Annealing on the Structural, Electrical, and Optical properties of DC Magnetron Sputtered Ta_2O_5 Films, Res. Lett. Mater. Sci., (2007), 1-5.
17. A.P. Huang, Z.C. Yang, Paul K. Chiu in: Paul K. Chiu (Eds.), Hafnium based high-k gate dielectrics, Adv. Sol. State Cir. Tech., INTECH, Croatia, (2010) 446.
18. S.V. Jagadeesh Chandra a, Jin-Sung Kim, Kyung-Won Moon and Chel-Jong Choi, Effect of post-metallization annealing on structural and electrical properties of Ge metal-oxide-semiconductor (MOS) capacitors with Pt/HfO_2 gate stack, Microelectron. Engg., **89** (2012) 76-79.
19. S.V. Jagadeesh Chandra, M.R. Jeong, K.H. Shim, H.B. Hong, S.H. Lee, K.S. Ahn, C.J. Choi, Effective metal work function of Pt gate electrode in Ge metal oxide semiconductor (MOS) device with HfO_2 gate dielectric, J. Electrochem. Soc., **157 (5)**, (2010) H546-H550.
20. S.V. Jagadeesh Chandra, E. Fortunato, R. Martins, C.J. Choi, Modulations in effective work function of platinum gate electrode in metal-oxide-semiconductor devices, Thin Solid Films, **520** (2012) 4556-4558.
21. M.Hasan, M.S. Jo, Md. S. Rahman, H.Choi, S. Heo, H. Hwangz, "Electrical Characteristics of $LaAlO_3$ Gate Dielectrics Prepared by High-Pressure Hydrogen Post-Deposition Annealing, Electrochem. Solid State Lett., **9 (11)** (2006) F77-F79.